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Wafer-level Packaging (WLP) Reliability and Stress Driven Failure Modes

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Abstract

Wafer-Level Packages (WLP) offers an excellent solution to meet the growing demand for small, thin, and fast electronic products. Due to its low cost and high performance, WLP has a strong position in the handheld and mobile electronic system applications. However, the Fan-in/Fan-out WLP technologies shows a growing interest in the aerospace and defense applications. Thermo-mechanic reliability of WLP remains a major challenge for higher I/O and larger die in the support of Defense and Aerospace electronic systems. In this work, we provide a comprehensive overview of WLP based on stress test's driven reliability, associate's failure modes, detailed physics of failures, and fundamentals of board level failure mechanism.

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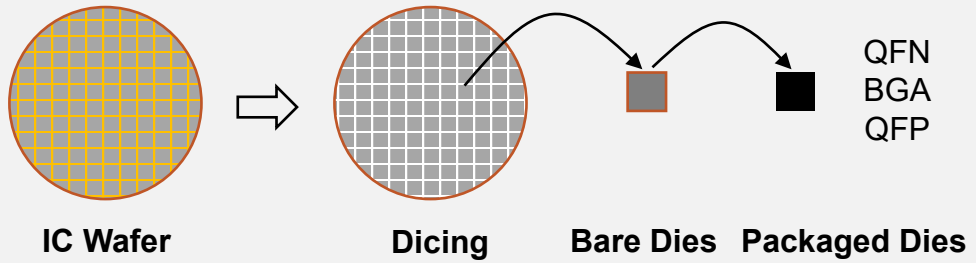
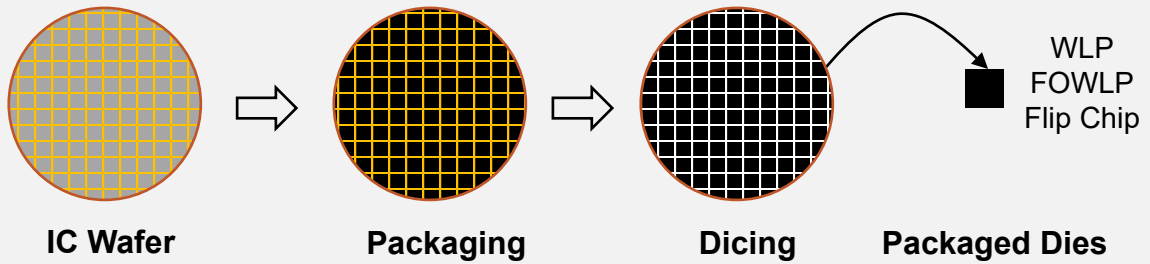
Outlines

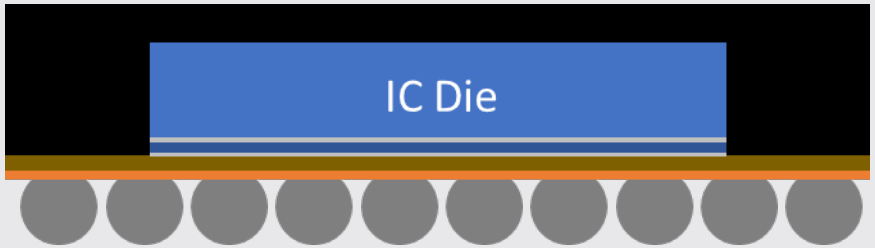
- Overview of Wafer-level Packaging (WLP)
- Physics of Failures and Board-level Interconnects Stress Fundamentals
- Stress Test's Drive Failure Modes
- Board Level Reliability Improvements
- Summary

Wafer-level Packaging (WLP) - Overview

Packaging Technologies	Packaging Flow
Conventional Packaging	
Wafer-level Packaging	

WLP Benefits

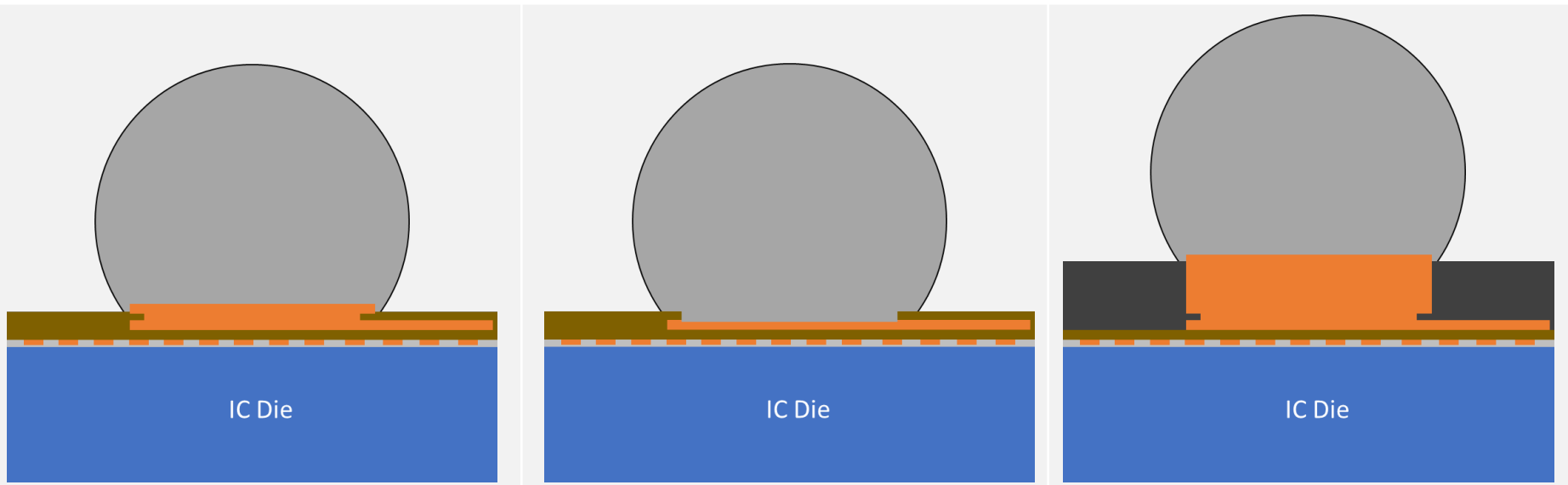
- ✓ Low-Cost Packaging
- ✓ Smaller Footprints
- ✓ Enable High Density Integration
- ✓ Improved Board-level Manufacturability due Bumps Pitch Fan-out
- ✓ Higher Electrical Performance
- ✓ Improved Reliability

Wafer-level Packaging	Fan-In WLP	Fan-Out WLP
		

Wafer-level Packaging (WLP) – Manufacturing Flow

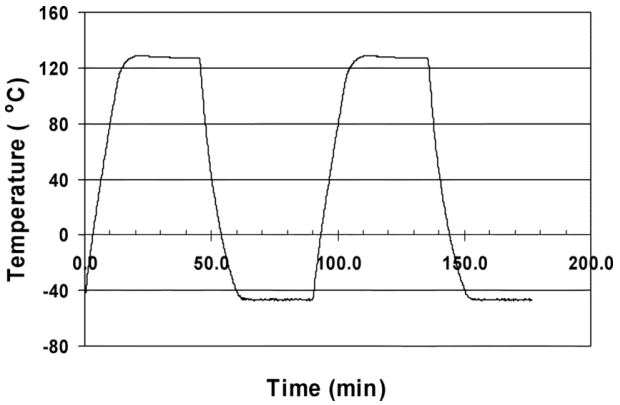
IC Wafer with Al Pad Open → Dielectric Layer-1 Coating → RDL Metal Plating → Dielectric Layer-2 Coating → UBM Metal Plating → Bumping → Backgrinding & Thinning → Dicing

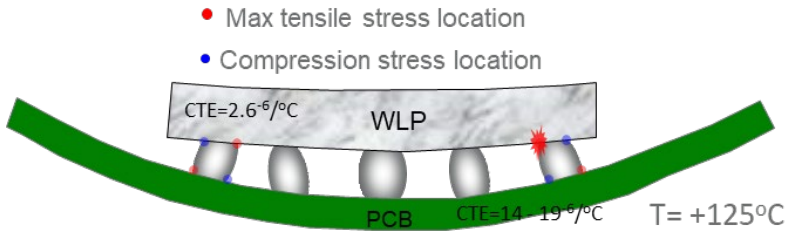
WLP Structural Variations	WLP - A	WLP - B	WLP - C



Wafer-level Packaging (WLP) – Reliability Fundamentals

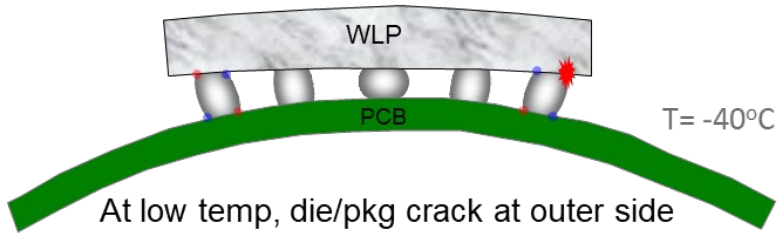
Temperature Cycling



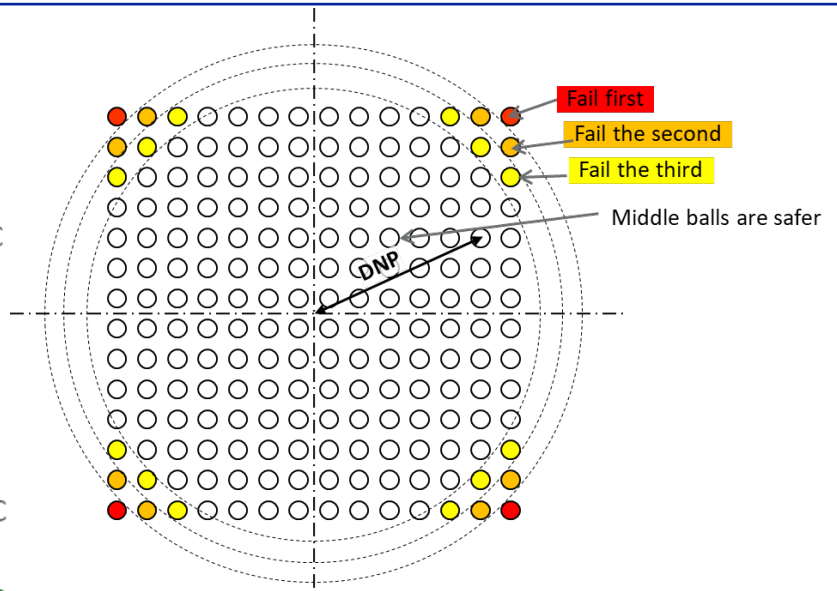


Solder joint crack at high temp at inner side

TC Test



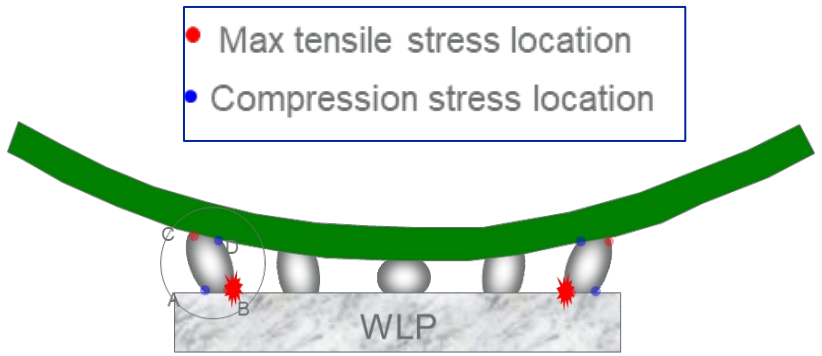
At low temp, die/pkg crack at outer side



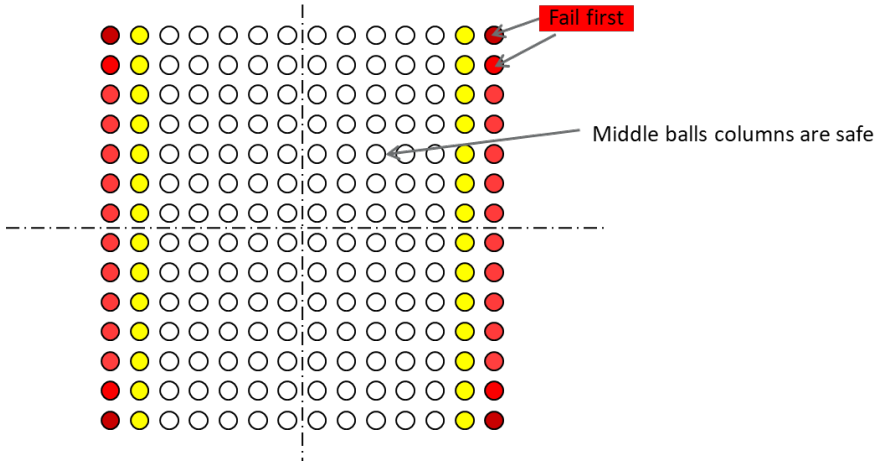
Shock & Bend

Drop Test @
1500Gs / 2900Gs
0.5 ms duration

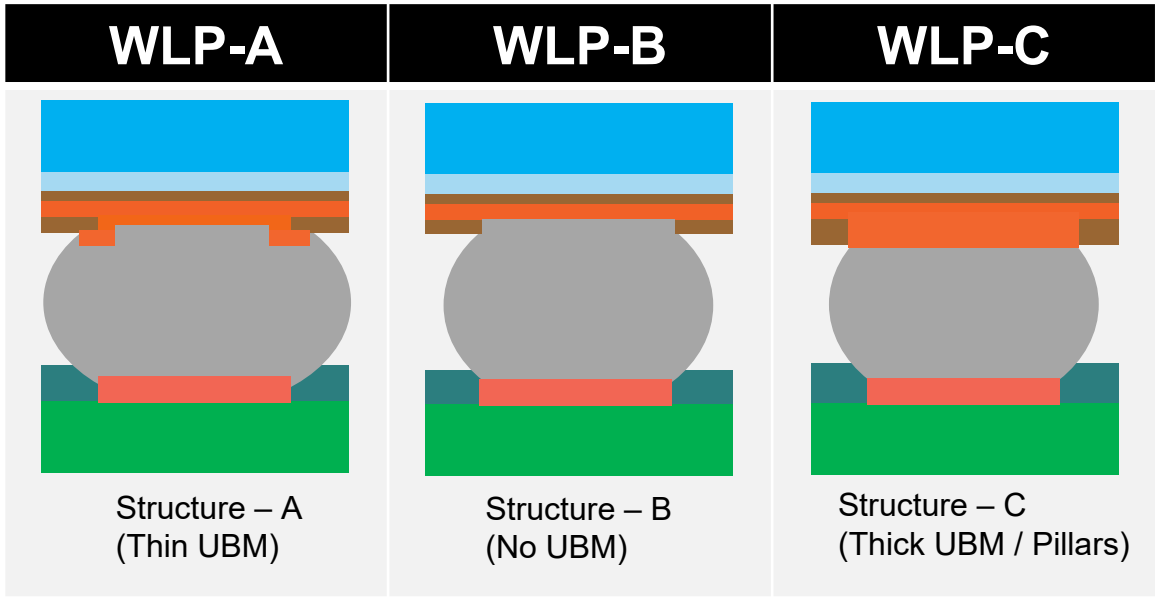
Cyclic Bend @ 1Hz

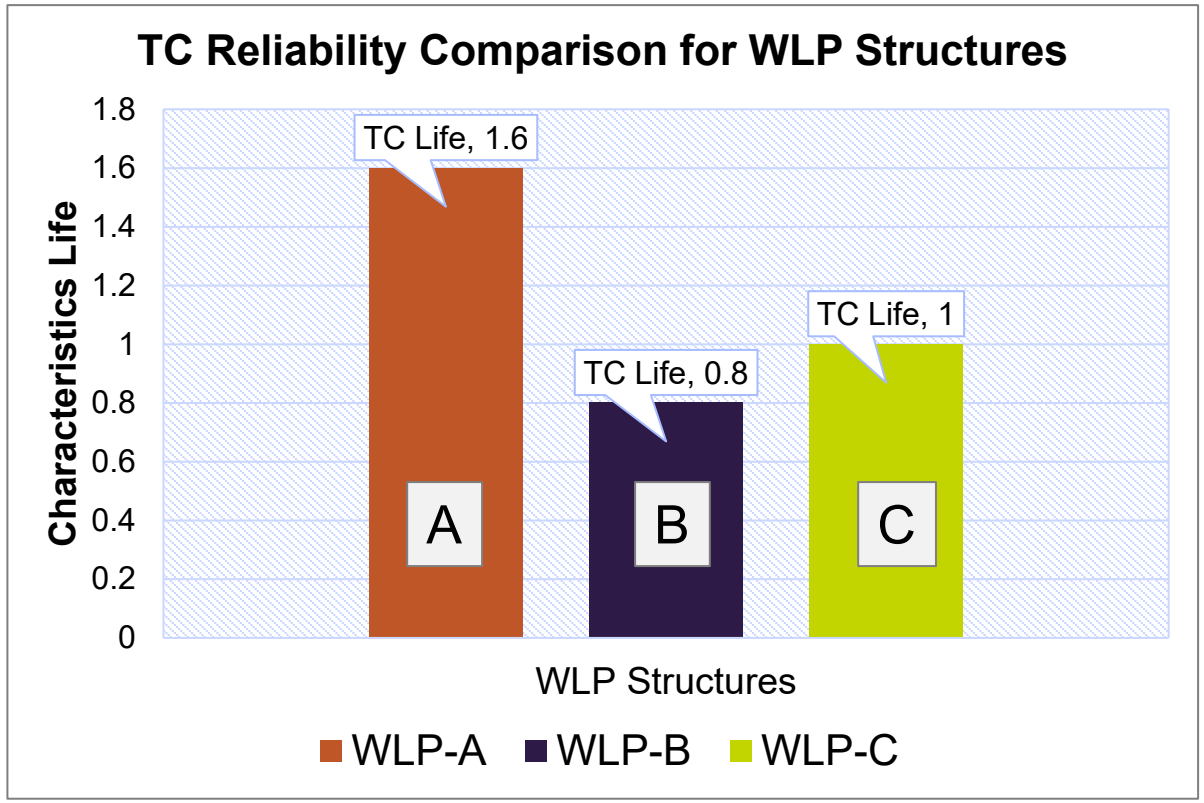


Shock / Cyclic Bend Test



Wafer-level Packaging (WLP) – Reliability Assessments





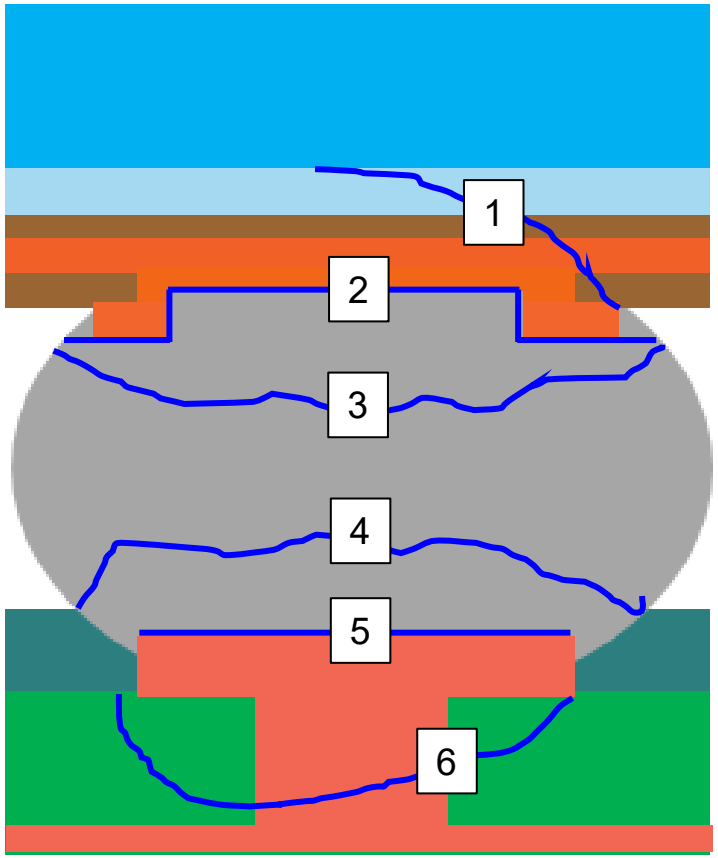
For the Same Die/Package Size:

- WLP-A has 60% Higher TC Life Compared to WLP-C
- WLP-C has 20% Higher TC Life Compared to WLP-B

Temperature Cycling Test Data
-40°C / +125°C, 1cph

Reference: M. S. K. Rahim, Tiao Zhou, Xuejun Fan and G. Rupp, "Board level temperature cycling study of large array Wafer Level Package," *2009 59th Electronic Components and Technology Conference*, San Diego, CA, USA, 2009, pp. 898-902, doi: 10.1109/ECTC.2009.5074119.

Wafer-level Packaging (WLP) – Structural Failure Modes



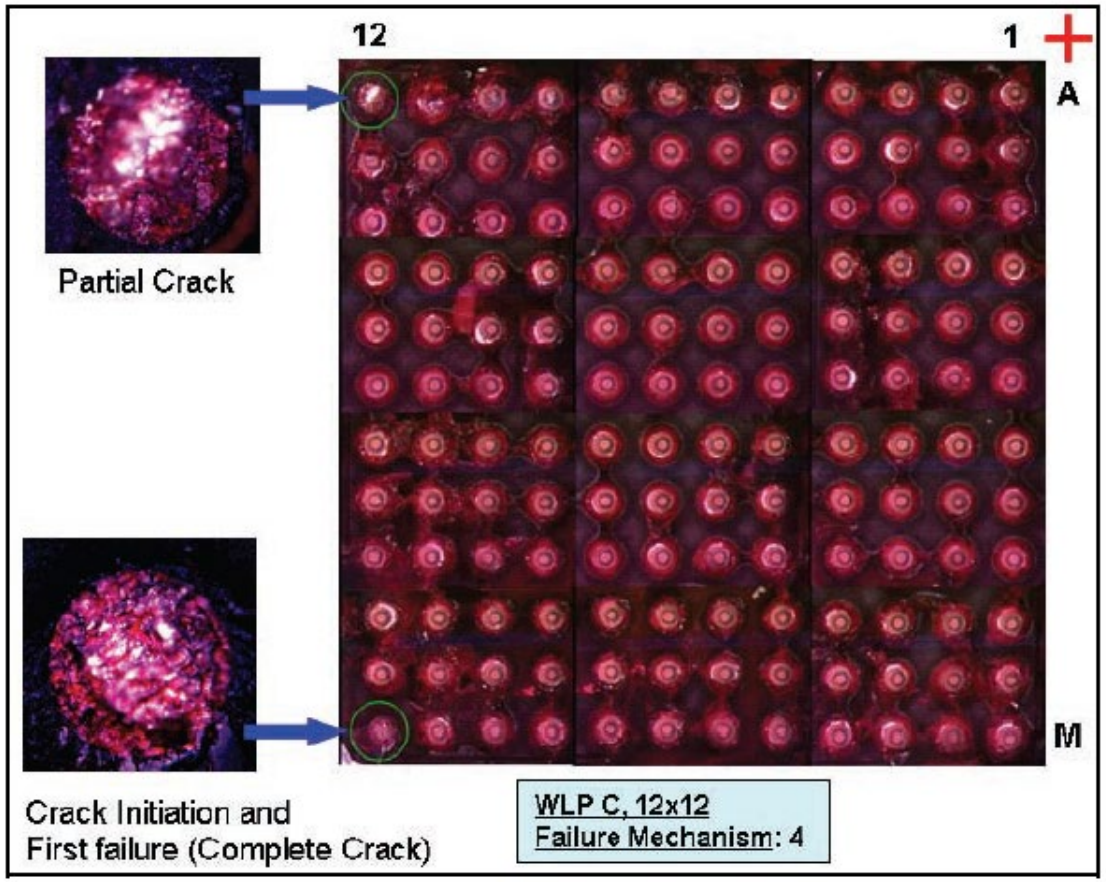
Failure Modes	Failure Mechanism
1	Die / Package Crack
2	IMC Crack (Package Side)
3	Bulk Solder Crack (Package Side)
4	Bulk Solder Crack (Substrate Side)
5	IMC Crack (Substrate Side)
6	Substrate Crack (Pad Crater, Micro-via Crack)

- Thermo-mechanical and Shock / Drop Stress-Related Failures
- Failure Mode 3 is the Primary Failure Mechanism for a Good Process

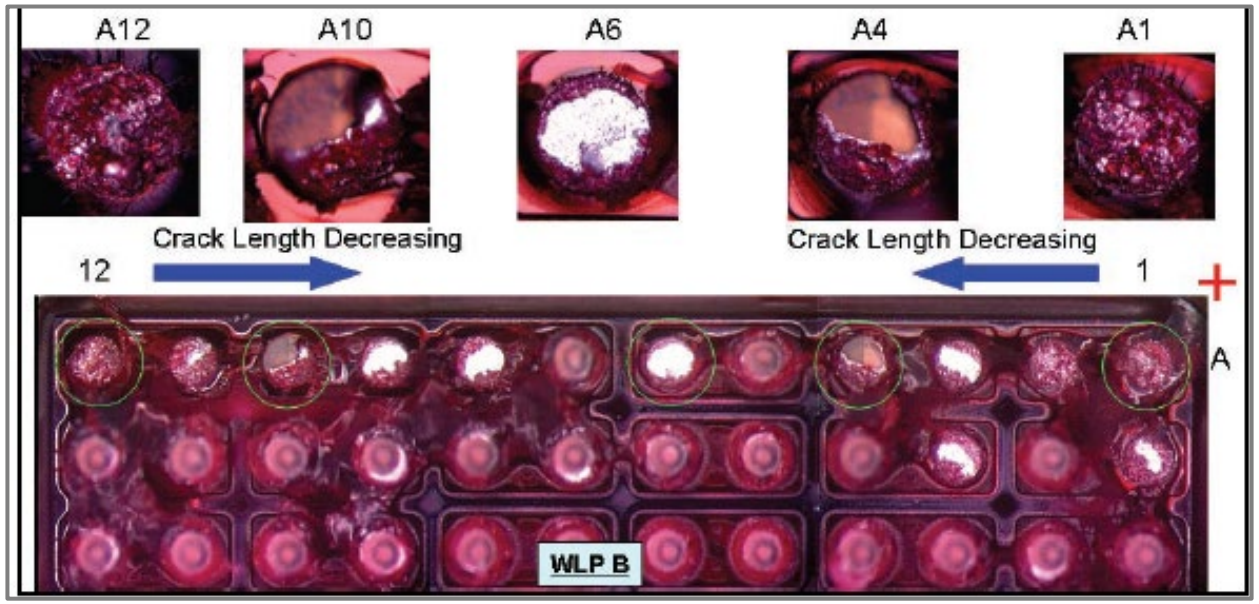
Reference: M. S. K. Rahim, Tiao Zhou, Xuejun Fan and G. Rupp, "Board level temperature cycling study of large array Wafer Level Package," *2009 59th Electronic Components and Technology Conference*, San Diego, CA, USA, 2009, pp. 898-902, doi: 10.1109/ECTC.2009.5074119.

Wafer-level Packaging (WLP) – TC Induced Failure Initiation

Dye & Pry Failure Analysis Technique



Sample Taken Out Immediately after Failures



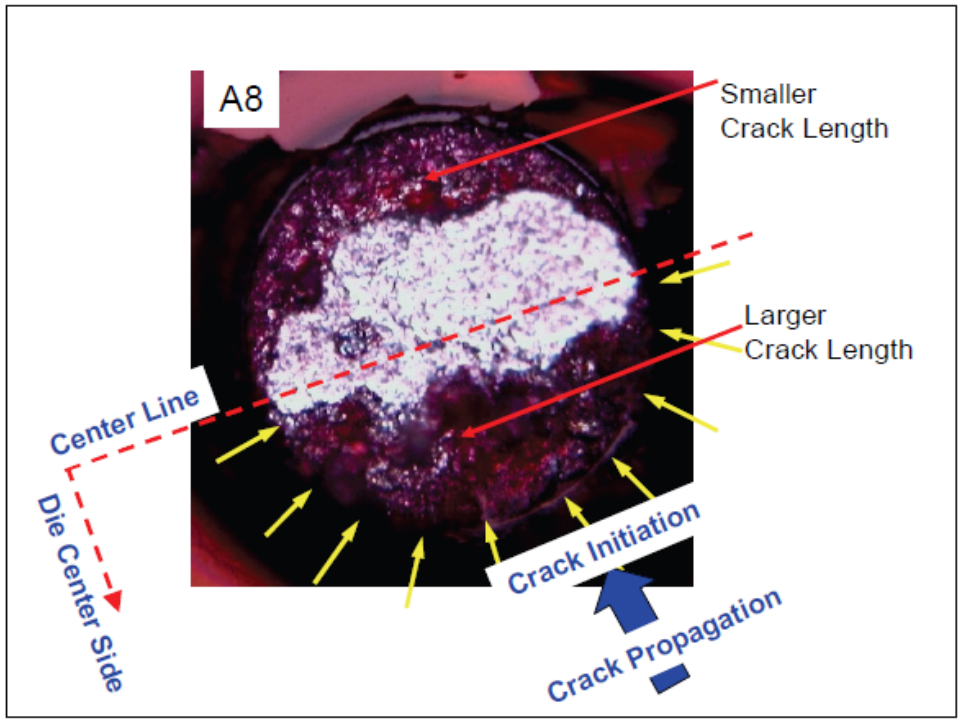
Sample Taken Out after Prolonged TC Test

- Corner Solder Joints Failed First
- Solder Joint Crack Propagates towards the Center of the Package

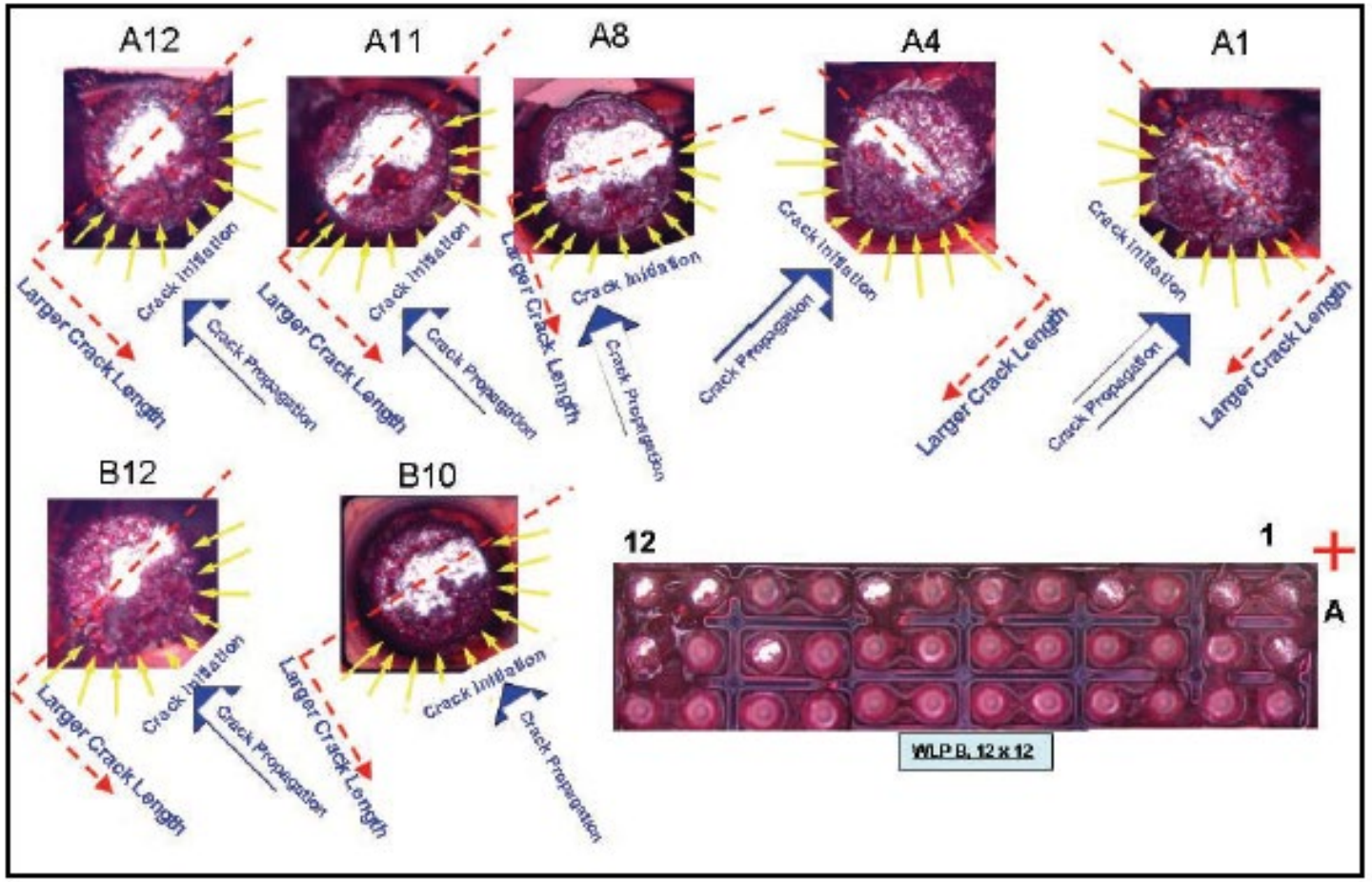
Reference: M. S. K. Rahim, Tiao Zhou, Xuejun Fan and G. Rupp, "Board level temperature cycling study of large array Wafer Level Package," *2009 59th Electronic Components and Technology Conference*, San Diego, CA, USA, 2009, pp. 898-902, doi: 10.1109/ECTC.2009.5074119.

Wafer-level Packaging (WLP) – TC Induced Failure Initiation

Dye & Pry Failure Analysis Technique



Solder Joint Crack Initiation Mechanism

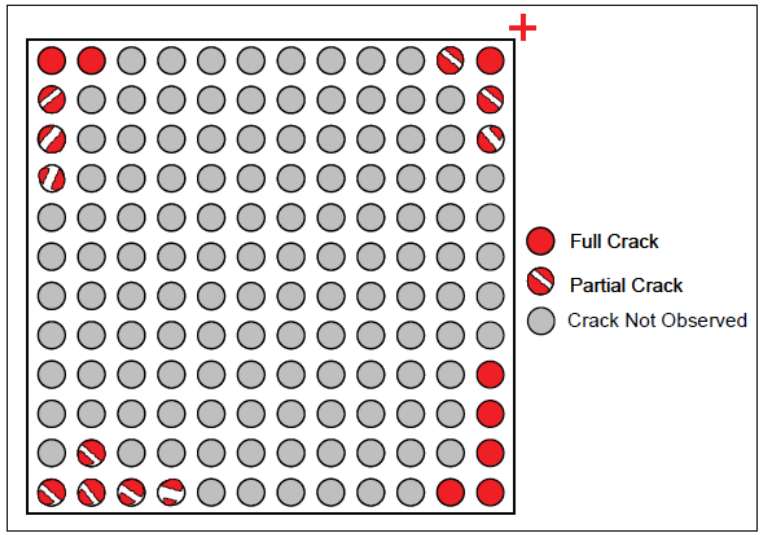


- Solder Joint Crack Initiate at the Center side of the Joint, where Higher Tensile Stress Developed during Substrate Thermal Mismatch

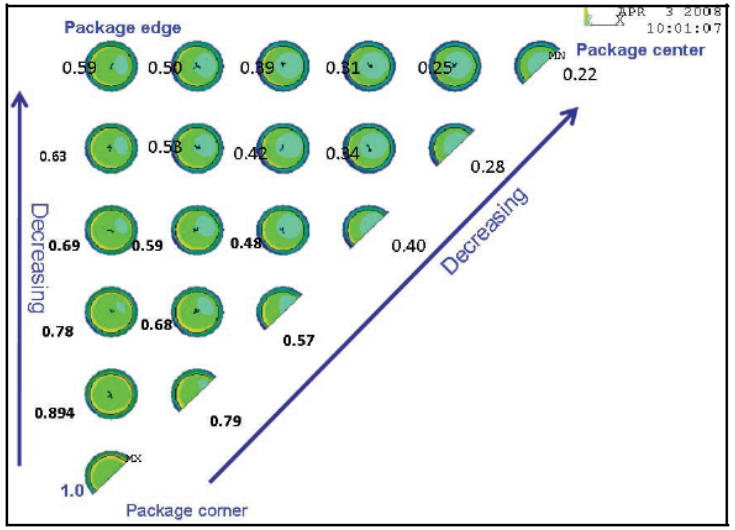
Reference: M. S. K. Rahim, Tiao Zhou, Xuejun Fan and G. Rupp, "Board level temperature cycling study of large array Wafer Level Package," *2009 59th Electronic Components and Technology Conference*, San Diego, CA, USA, 2009, pp. 898-902, doi: 10.1109/ECTC.2009.5074119.

Wafer-level Packaging (WLP) – TC Induced Failure Initiation

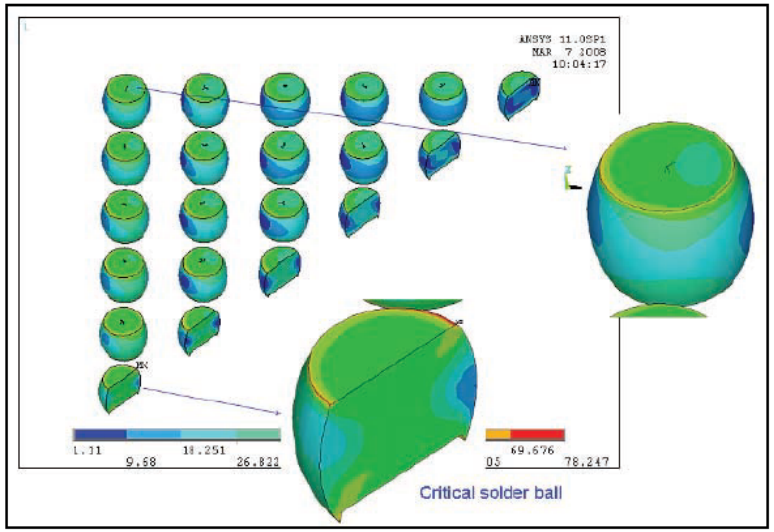
Simulation of TC Data with Finite Element Analysis



Complete Crack Map
after Prolonged TC Test



Inelastic Energy Density Contour
for Corner Solder Joint

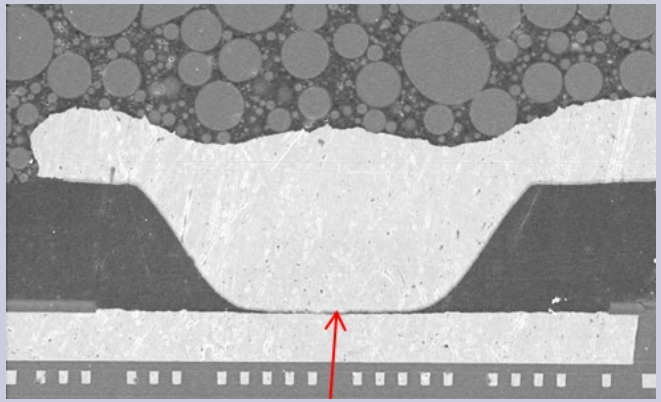
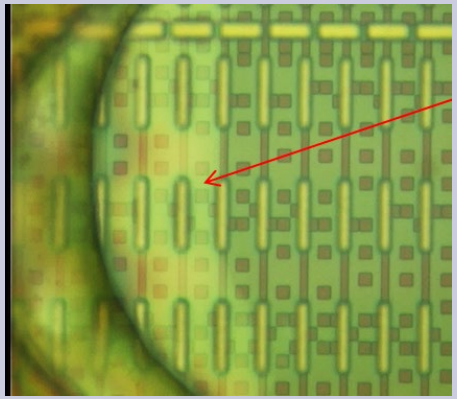
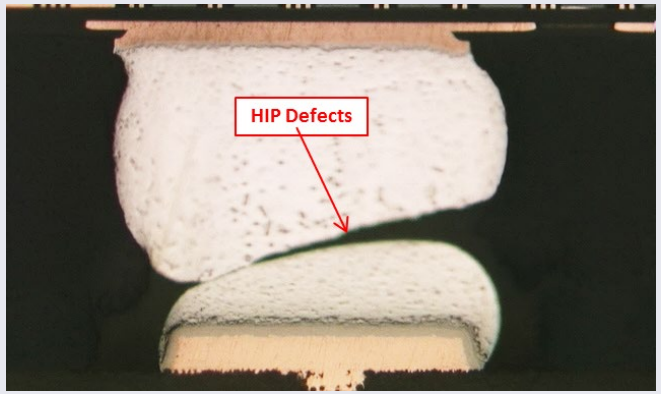


Von Mises Stress in Solder Balls
for Identifying the Critical Ball

- TC Test Failures / Crack Maps Correlates very well with Finite Element Analysis Data

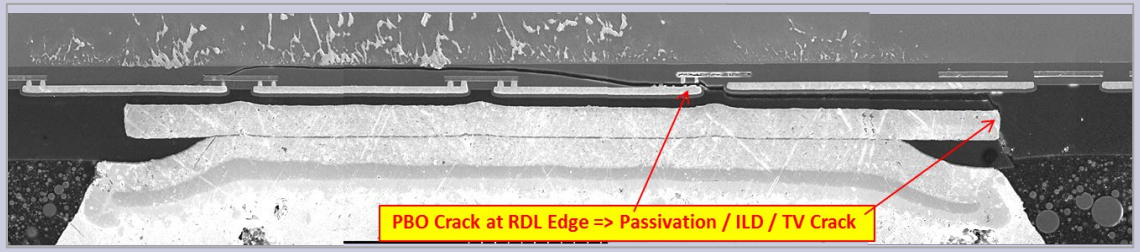
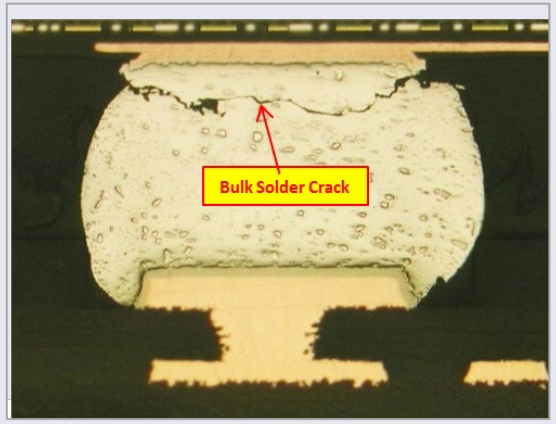
Reference: M. S. K. Rahim, Tiao Zhou, Xuejun Fan and G. Rupp, "Board level temperature cycling study of large array Wafer Level Package," *2009 59th Electronic Components and Technology Conference*, San Diego, CA, USA, 2009, pp. 898-902, doi: 10.1109/ECTC.2009.5074119.

Wafer-level Packaging (WLP) – Process Driven Time-0 Failure Mechanism

Failure Level	Failure Mechanism	Reliability Impacts
Die Level	 Dielectric Residue Trapped in Via Interface  Dielectric Delam	• Higher Via Resistance • Via Delam from Die metal • PI Delam can Cause Die Crack • Package Structural and Functional Failures
Interconnect Level	 Post-reflow Head in Pillow Defect (Solder Non-wet)	• Package Structural and Functional Failures

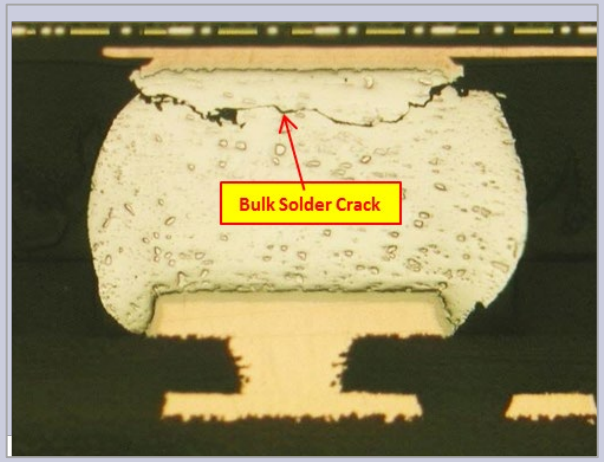
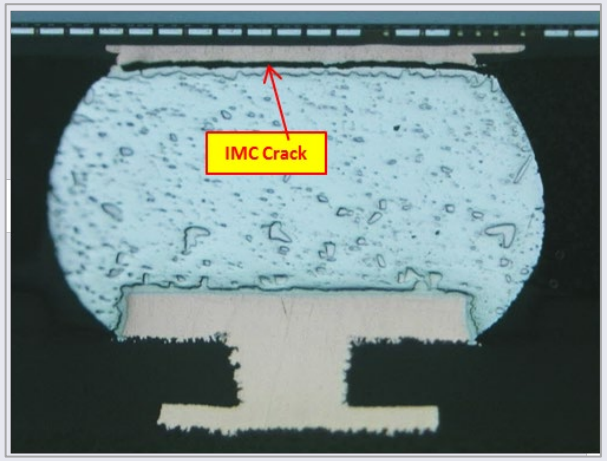
Reference: M. S. K. Rahim, Tiao Zhou, Xuejun Fan and G. Rupp, "Board level temperature cycling study of large array Wafer Level Package," *2009 59th Electronic Components and Technology Conference*, San Diego, CA, USA, 2009, pp. 898-902, doi: 10.1109/ECTC.2009.5074119.

Wafer-level Packaging (WLP) – Temperature Cycling Driven Failure Mechanism

Failure Level	Failure Mechanism	Reliability Impacts
Package Level	 Package Crack: PI Crack => ILD / Die Metal Crack	• Caused early failures • Not an expected failure mode
Interconnect Level	 Crack through Bulk Solder (Ductile Fracture)	• An expected failure mode • Can survive >1500 cycles for a good bumping and assembly process

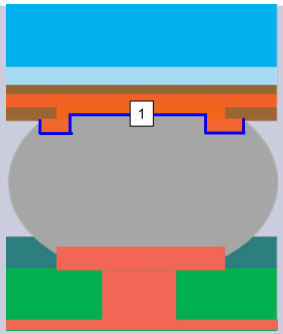
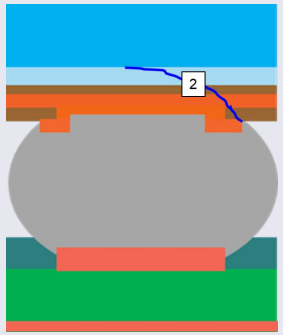
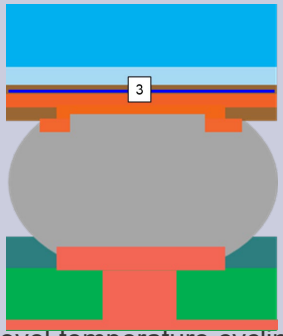
Reference: M. S. K. Rahim, Tiao Zhou, Xuejun Fan and G. Rupp, "Board level temperature cycling study of large array Wafer Level Package," *2009 59th Electronic Components and Technology Conference*, San Diego, CA, USA, 2009, pp. 898-902, doi: 10.1109/ECTC.2009.5074119.

Wafer-level Packaging (WLP) – Reliability Test Driven Failure Mechanisms

Reliability Test Conditions	Failure Mechanism	Reliability Impacts
Temperature Cycling (-55°C / +125°C)		• Crack through Bulk Solder (Ductile Fracture) • Intermittent failure • Little or No resistance change at RT probing
Drop Test (1500g, 0.5 ms)		• Crack through IMC Layer (Brittle Fracture) • Hard failure • Open or High Resistance at RT probing

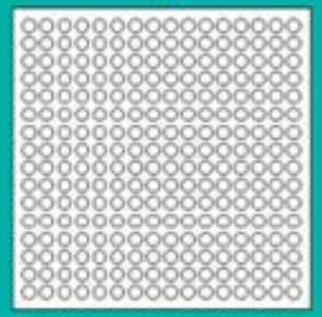
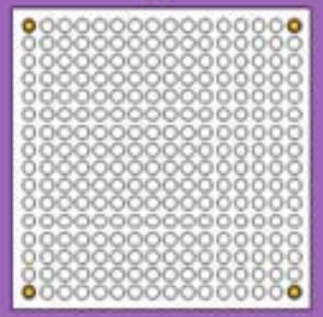
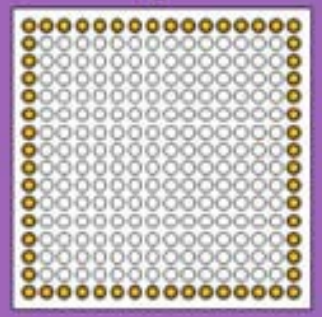
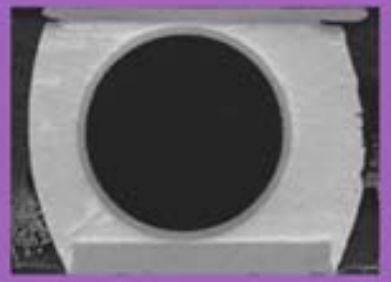
Reference: M. S. K. Rahim, Tiao Zhou, Xuejun Fan and G. Rupp, "Board level temperature cycling study of large array Wafer Level Package," *2009 59th Electronic Components and Technology Conference*, San Diego, CA, USA, 2009, pp. 898-902, doi: 10.1109/ECTC.2009.5074119.

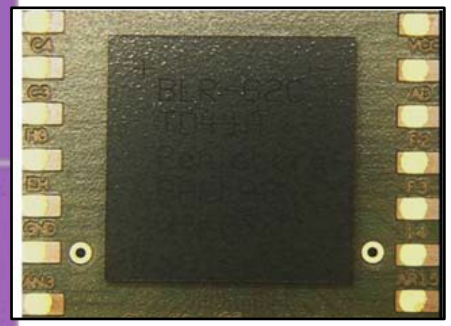
Wafer-level Packaging (WLP) – Reliability Test Driven Failure Mechanisms

Reliability Test Conditions	Failure Mechanism	Reliability Impacts
Drop Test (1500g, 0.5 ms)		• Solder Joint Crack through IMC Layer ▪ Intermetallic Fracture
MSL1 + Drop Test		• Package Crack: ▪ Dielectric / ILD / Die Metal Crack
MSL1 + HTS (150°C) + Drop Test		• Package Crack: ▪ Dielectric Delam from RDL Layer

Reference: M. S. K. Rahim, Tiao Zhou, Xuejun Fan and G. Rupp, "Board level temperature cycling study of large array Wafer Level Package," *2009 59th Electronic Components and Technology Conference*, San Diego, CA, USA, 2009, pp. 898-902, doi: 10.1109/ECTC.2009.5074119.

Wafer-level Packaging (WLP) – Solder Joint Reliability Improvements

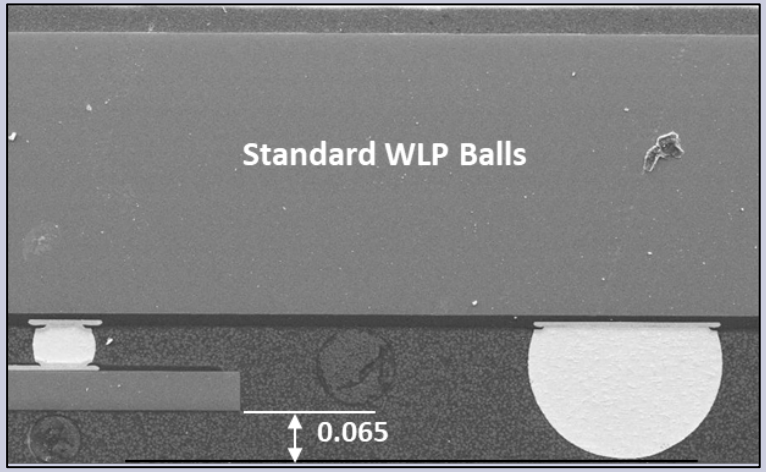
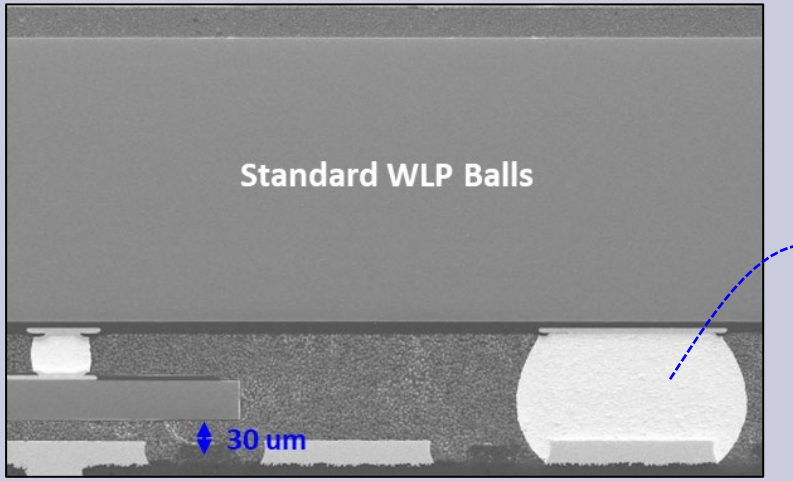
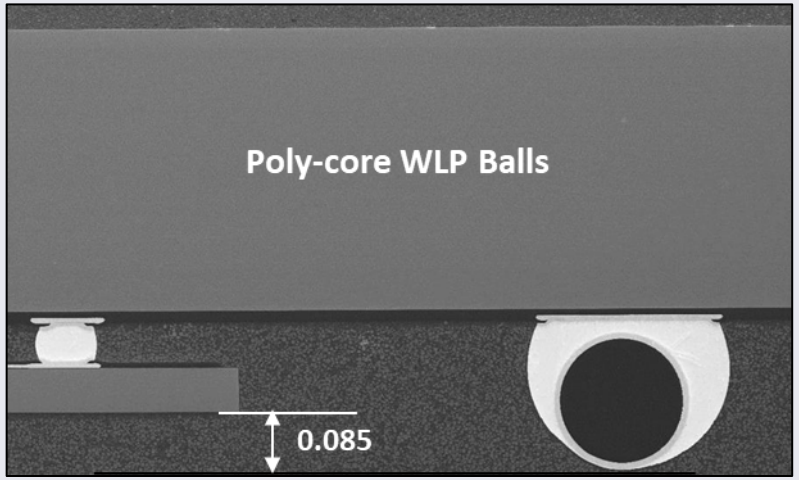
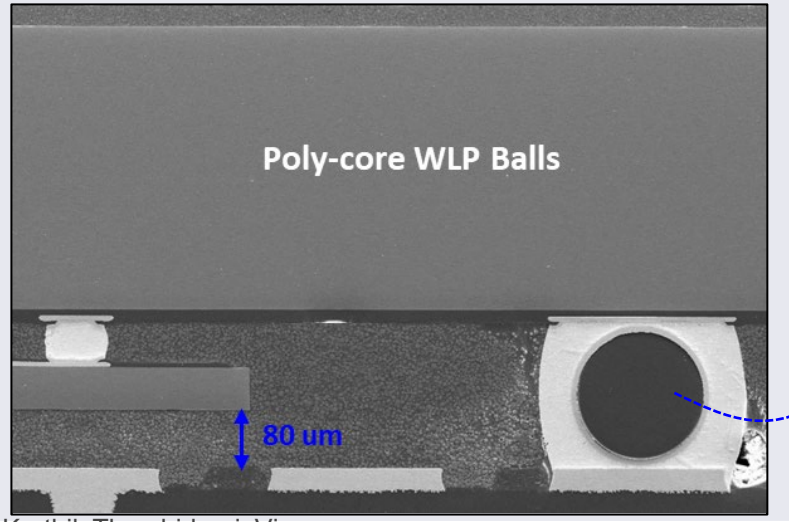
	A	B	C
WLP ball allocation		 or	
Solder joint shape			
Standoff	150 µm	200 µm	
Solder joint diameter	330 µm	275 µm for normal balls 300 µm for Plastic core balls	



Higher Stand-off
And
Higher Solder Joint Reliability

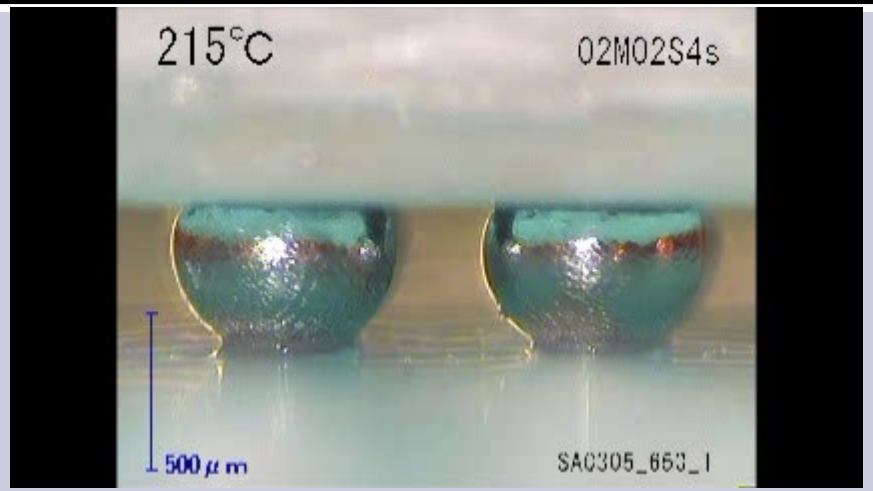
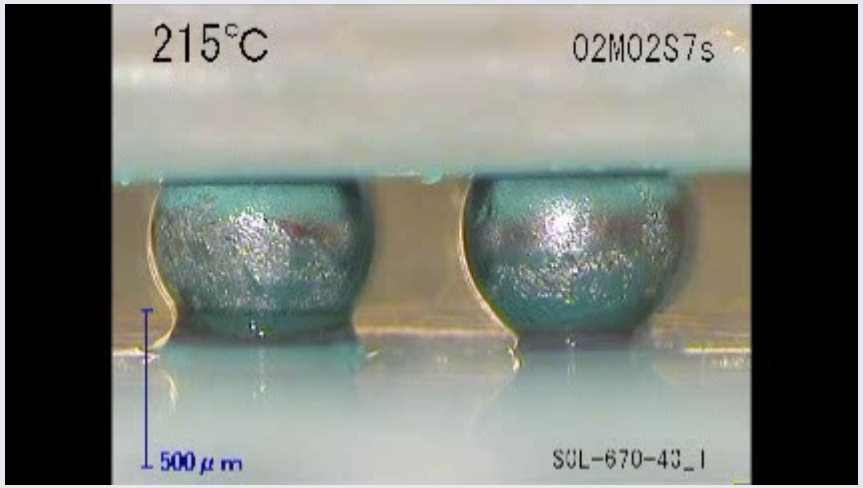
Reference: Development of Low Cost and High Pin Count Wafer Level Packaging by Karthik Thambidurai, Viren Khandekar, Tiao Zhou, Ph.D. and Kaysar Rahim, Maxim Integrated, Paper # 388, SMTA International Conference 2015, 27 September - 1 October 2015, Rosemont, IL, ISBN: 978-1-5108-1371-7"

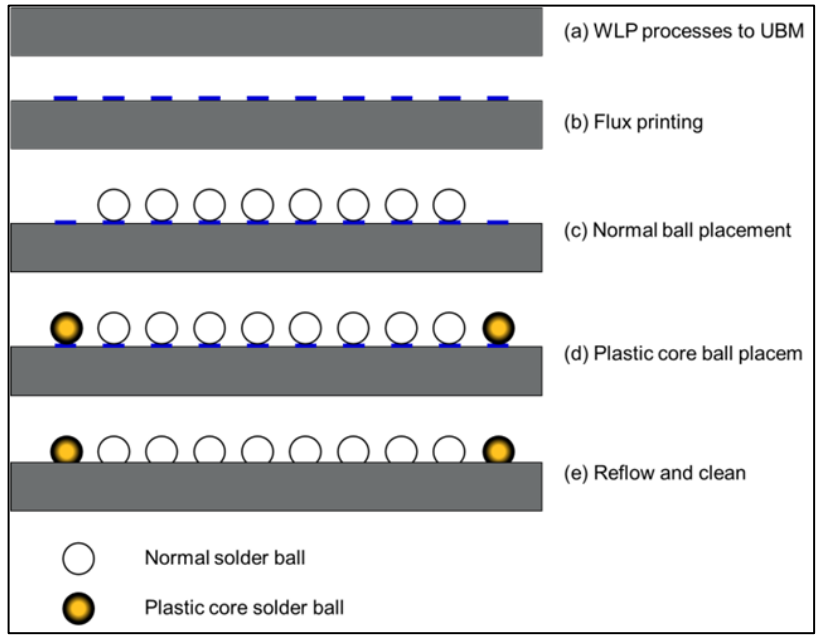
Wafer-level Packaging (WLP) – Solder Joint Reliability Improvements

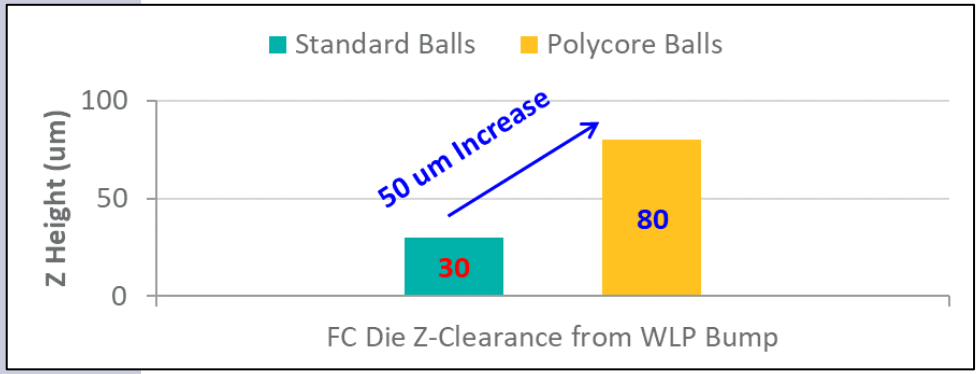
Bump Type	Pre-assembly	Post-assembly	Stand-off Increase
Standard WLP Bumps			**50 um Solder Stand-off Gain**
Poly-core WLP Bumps			

Reference: Development of Low Cost and High Pin Count Wafer Level Packaging by Karthik Thambidurai, Viren Khandekar, Tiao Zhou, Ph.D. and Kaysar Rahim, Maxim Integrated, Paper # 388, SMTA International Conference 2015, 27 September - 1 October 2015, Rosemont, IL, ISBN: 978-1-5108-1371-7"

Wafer-level Packaging (WLP) – Solder Joint Reliability Improvements

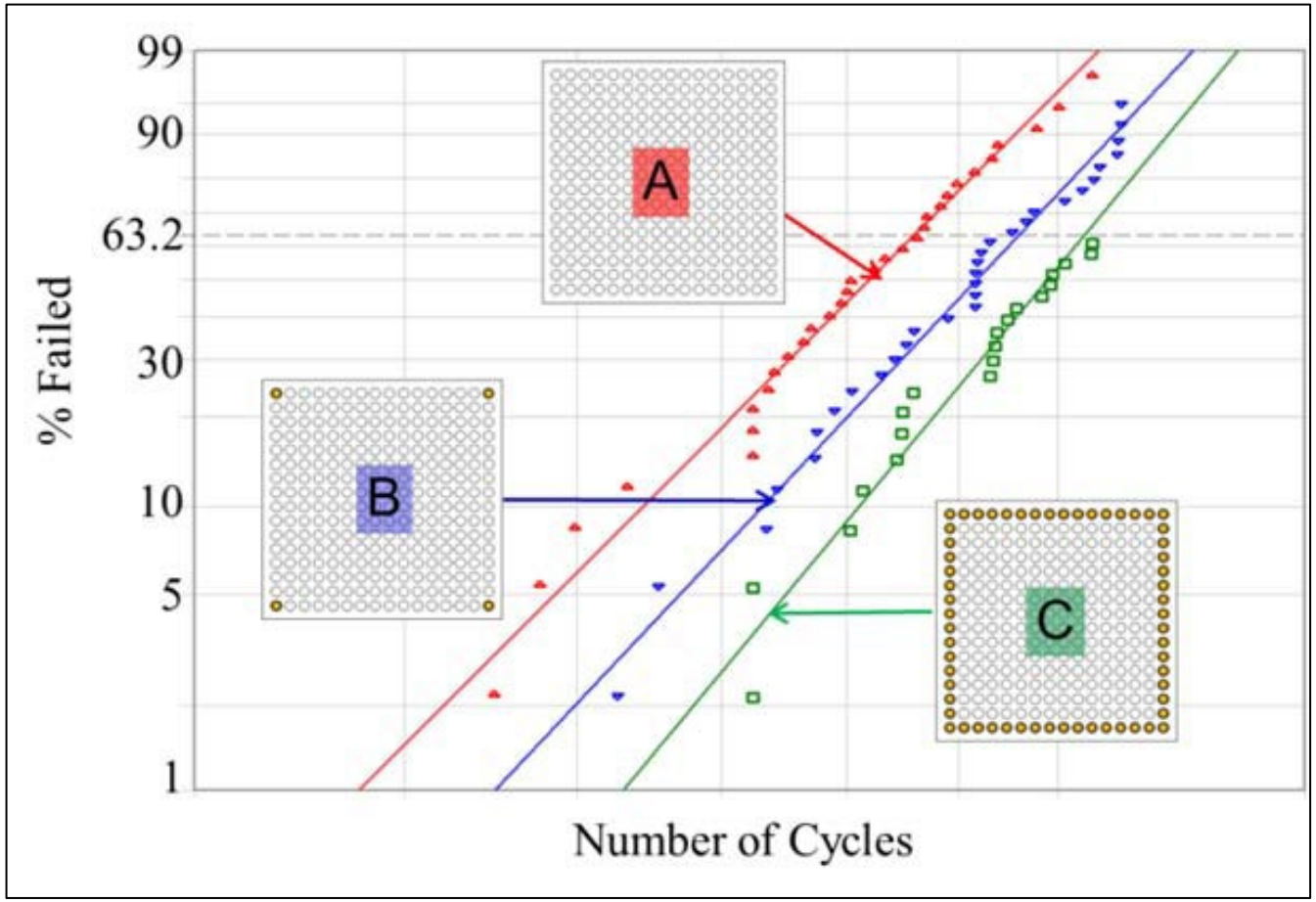
Bump Type	Bump Reflow during Assembly	Stand-off Increase
Standard WLP Bumps		**50 um Solder Stand-off Gain**
Poly-core WLP Bumps		

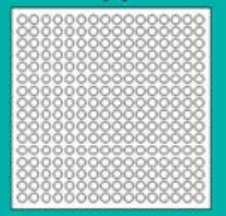
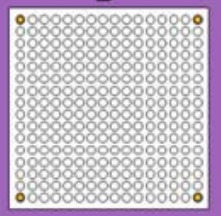
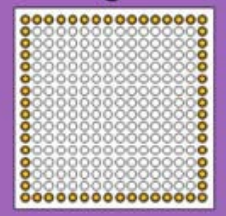


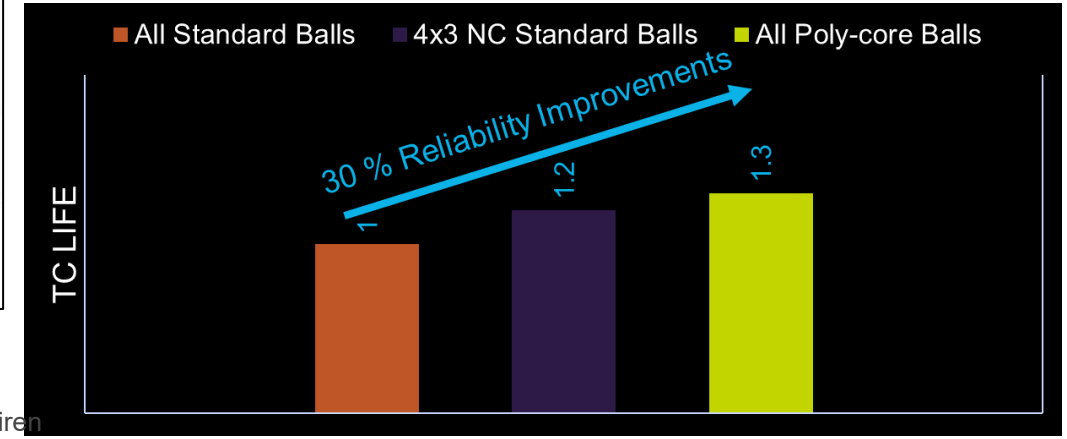


Reference: Development of Low Cost and High Pin Count Wafer Level Packaging by Karthik Thambidurai, Viren Khandekar, Tiao Zhou, Ph.D. and Kaysar Rahim, Maxim Integrated, Paper # 388, SMTA International Conference 2015, 27 September - 1 October 2015, Rosemont, IL, ISBN: 978-1-5108-1371-7"

Wafer-level Packaging (WLP) – Solder Joint Reliability Improvements



	A	B	C
WLP ball allocation		 or	
Solder joint shape			
Standoff	150 µm	200 µm	
Solder joint diameter	330 µm	275 µm for normal balls 300 µm for Plastic core balls	



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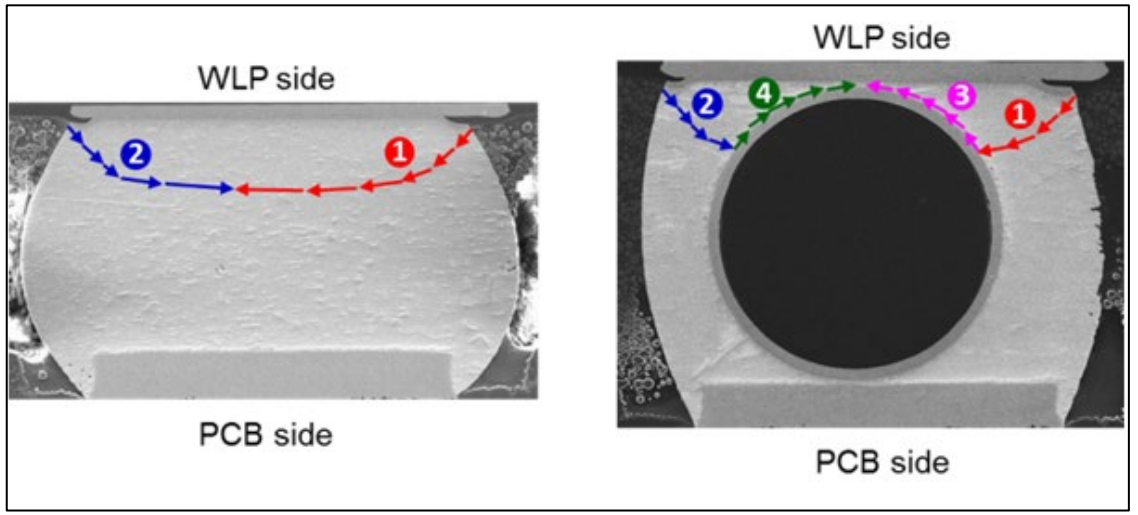
Wafer-level Packaging (WLP) – Solder Joint Reliability Improvements

Option	Corner Joint	Non-corner Joint
A		
B		
C		



- Poly-core Bumps Provided 30% Higher SJ TC Reliability
- Bulk Solder Crack at the Package Side is the Primary Failure Mechanism

Reference: Development of Low Cost and High Pin Count Wafer Level Packaging by Karthik Thambidurai, Viren Khandekar, Tiao Zhou, Ph.D. and Kaysar Rahim, Maxim Integrated, Paper # 388, SMTA International Conference 2015, 27 September - 1 October 2015, Rosemont, IL, ISBN: 978-1-5108-1371-7"

NORTHROP GRUMMAN

Summary

- FO-WLP has a Great Potential in Aerospace and Defense Applications
- Need to Address the Reliability Challenges for Higher I/O Count and Large Packages
- Need to Define the Right Stress Testing and Qualifications Requirements for the Defense and Aerospace Applications
- Need to Understand the Fundamentals of the Failure Mechanisms Associated with Field Stressing
- Need to Define the Design for Reliability (DFR) Aligned with Defense and Aerospace Applications