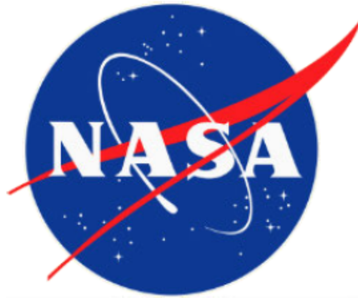

Reliability and Quality of Off-chip Interconnects in Advanced Packages in Perspective of High-Reliability Space Applications

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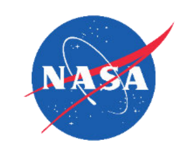
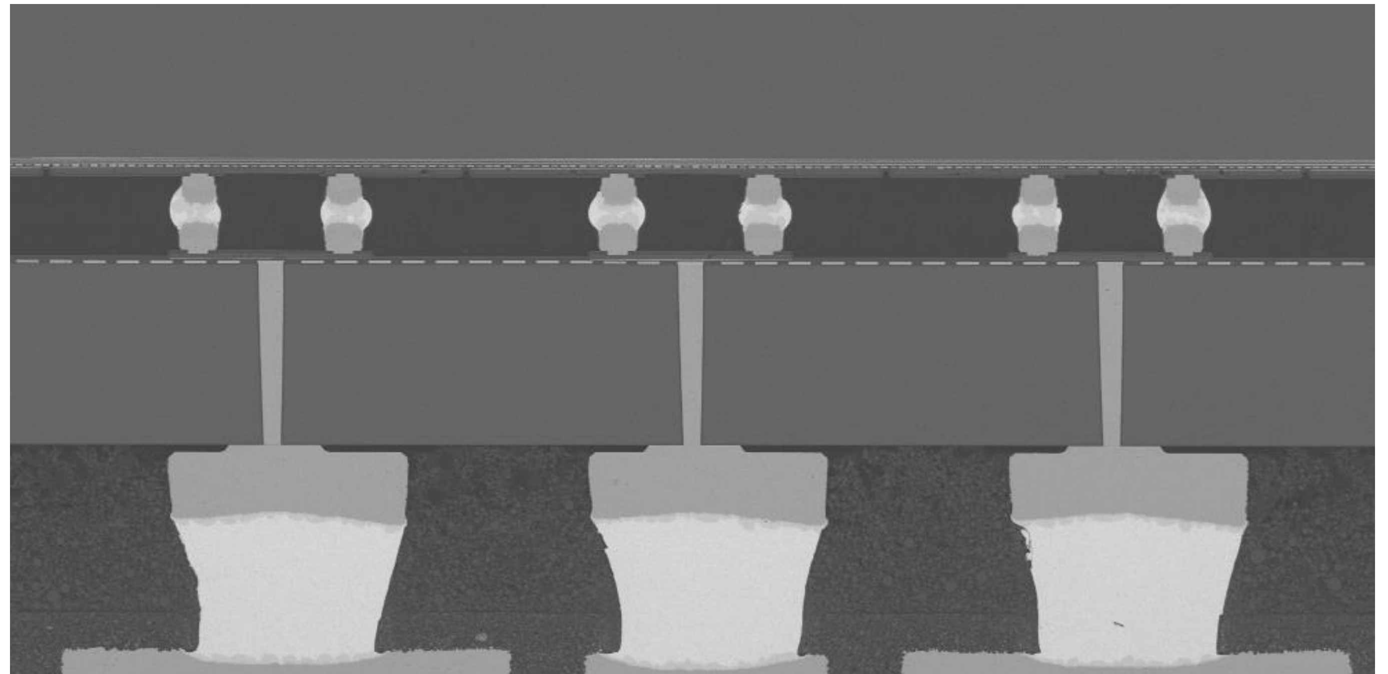


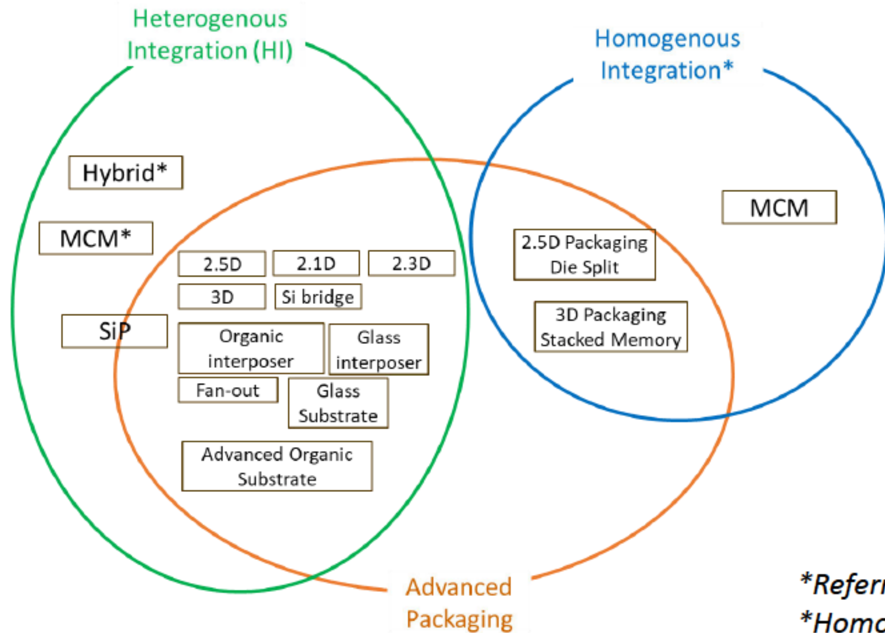
Purpose of The Presentation

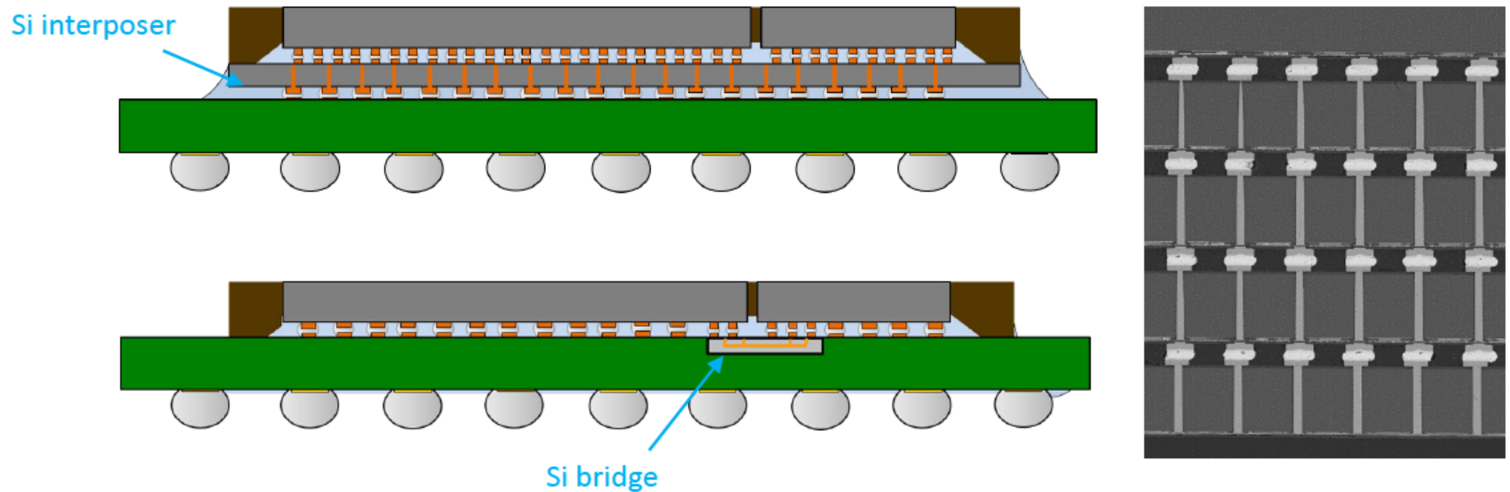
- Debrief the community on Advanced Packaging
  - Focus on off-chip interconnect
  - Manufacturing process and packaging materials
  - Reliability and quality implications
  - Share thoughts after trying to protype Advanced Packages for R&D tasks.



Advanced Packaging

- "Advanced Packaging"
  - Covers a broad range of packaging architecture
  - '2.5/3D', '2DS', '2.xD', 'Heterogenous Integration', etc...
- Packaging architecture capable of integrating multiple dies in one package with very high-density interconnect.
  - Large number of interconnect across very short distance between dies.
    - Laterally : with interconnect density far beyond organic substrate (comparable to BEOL).
    - Vertically : TSV (Through Silicon Via)





Referring hybrid and MCMs as HI doesn't match the commonly used context.

Homogenous Integration is not commonly used word. It's used here as the opposing concept to the HI.

There are many packaging architectures

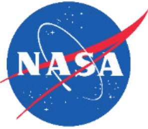
- Each trade name should be considered as a unique architecture.
- Same architecture can have different assembly process flow and materials.

TSMC	CoWoS-S	Lateral: Si Interposer. (2.5D)
	CoWoS-R	Lateral: RDL interposer
	CoWoS-L	Lateral : Organic interposer, embedded with Si bridge that has TSV
	InFO_oS	Lateral : Fan-out. No microbump. Has C4 and substrate.
	SoIC-CoW	Vertical : Some active dies are stacked (3D) with Chip-to-Wafer (C2W) hybrid bonding instead of microbump. Lateral : Si interposer.
	SoIC-WoW	Vertical : Some active dies are stacked (3D) with Wafer-to-Wafer (W2W) hybrid bonding instead of microbump. Lateral : Si interposer.
Intel	EMIB	Lateral : Si bridges (no TSV) embedded inside organic substrate
	Foveros	Vertical: Active dies stacked together (3D). Bottom die can be replaced with Si interposer (2.5D).
	Co-EMIB/EMIB 3.5D	Vertical: Active dies stacked together. (Foveros 3D) Lateral : 3D dies latterally integrated with Si bridge. (EMIB)
Samsung	I-CubeS	Lateral : Si Interposer like CoWoS-S. (2.5D)
	I-CubeE	Lateral : RDL interposer embedded with Si bridge that has TSV
	H-Cube	Lateral : Si Interposer like I-CubeS, with additional intermediate substrate between interposer and bottom substrate
	X-Cube	Vertical : Active dies are stacked together (3D), either via microbump or hybrid bonding.
ASE	FOCoS-CF	Lateral: Fan-out. No microbump. Has C4 and substrate.
	FOCoS-CL	Lateral : Fan-out. Has microbump.
	FOCoS-Bridge	Lateral : Fan-out with Si bridge (No TSV). Has microbump.
Amkor	SWIFT	Lateral : Fan-out. Has microbump. Can support package-on-package.

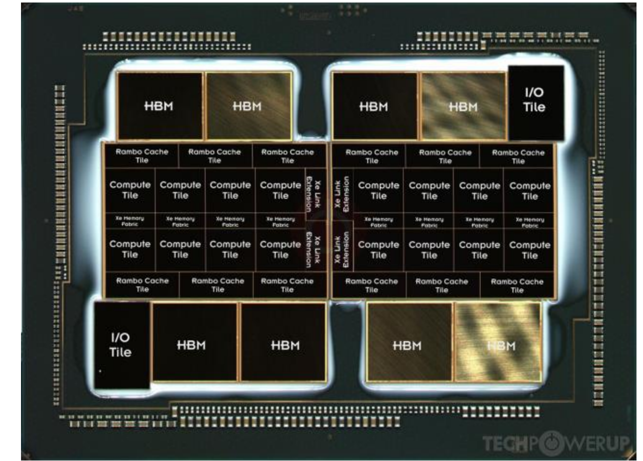
(?)

Same Architecture.

Depending on the design choices, can result in the same/similar architecture.



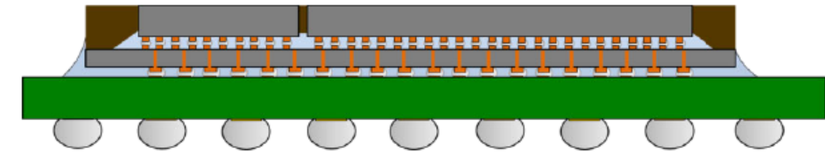
Some of Remarks Relevant for High-rel

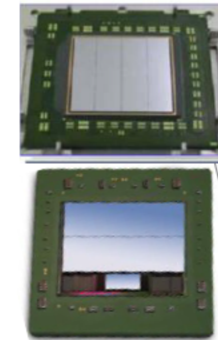


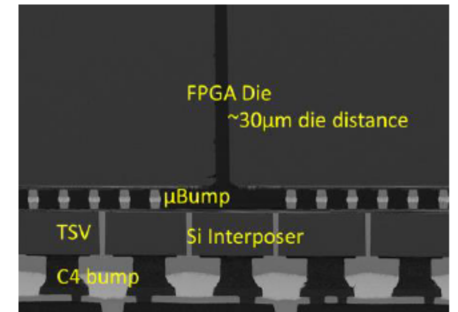
- Lot code
  - Same lot code ≠ homogneous.
  - 2D barcode may be used instead of lot code.
  - Even for the future mil-spec parts.
  - COTS part upscreening will be challenging.
- KGD
  - KGD are integrated together… But KGD may not exactly be "KGD".
- Traceability
  - Most Advanced Packages currently in the market are produced by manufactures vertically integrated. Practices are developed around accordingly.
  - When dies from multiple manufactures are integrated together, the traditional mil/space approach may not be feasible.
- HVM
  - Practices are developed around HVM.
  - Requires expensive infrastructure that typical OSATs do not have.
  - There are DoD activities to enable low-volume high-mix domestically.
    - SHIP, RESHAPE

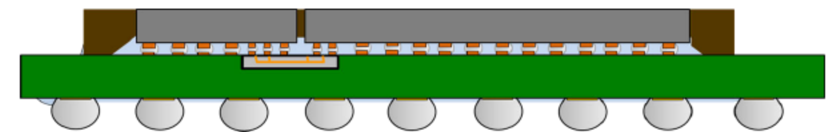
Examples

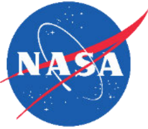
1. FPGA
   - Xilinx commercial FPGA
     - Some of V7, Kintex Ultrascale, Virtex Ultrascale, Versal
     - CoWoS-S (“2.5D”).
     - Si interposer only provides interconnect.
     - Mostly Die Split for yield (Homegenous).
     - Some are HI. (FPGA + Transceiver)
   - Intel FPGA
     - Stratix 10, Agilex 7 (F, I, M), Agilex 9 Direct-RF
     - Intel EMIB.
     - Si bridge (doesn’t have TSV) embedded in HBDU substrate.
     - µbumps have tight pitch above Si bridge.



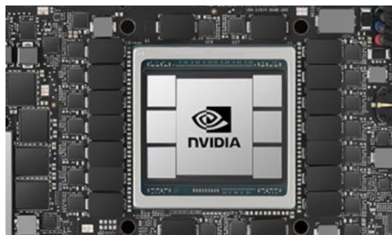


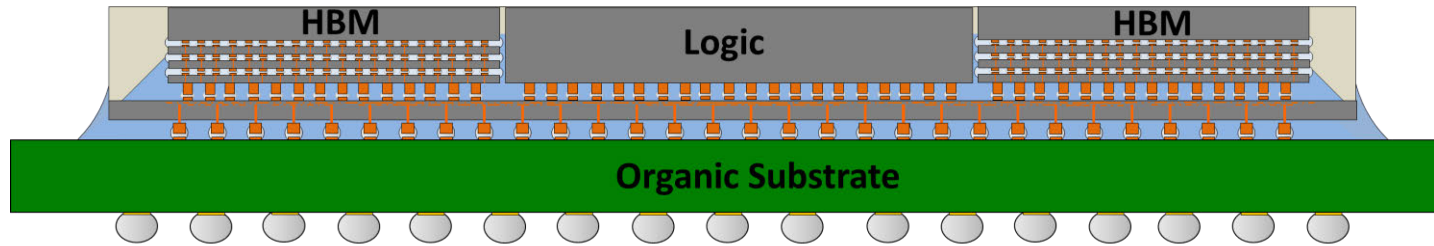


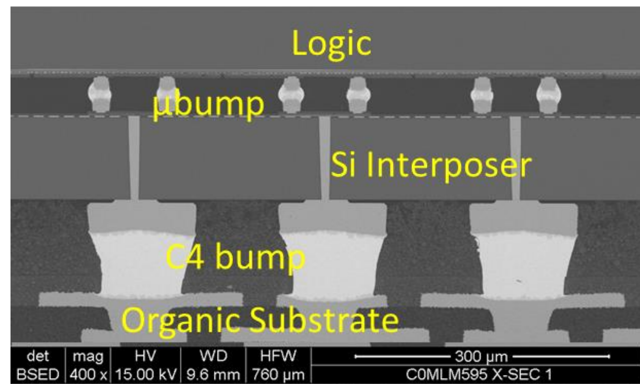


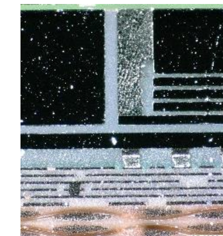


2. GPU/AI accelerator

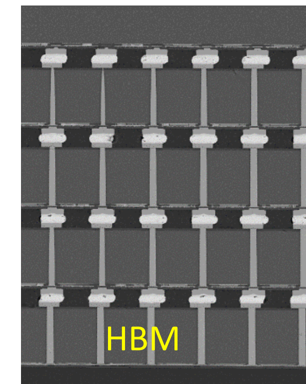




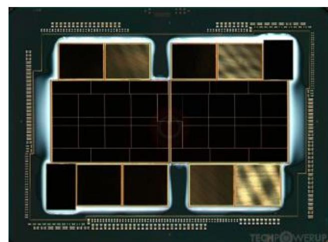


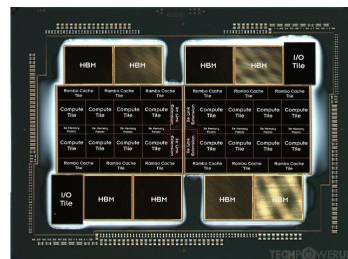


HBM placed 80µm from logic



Nvidia GV100

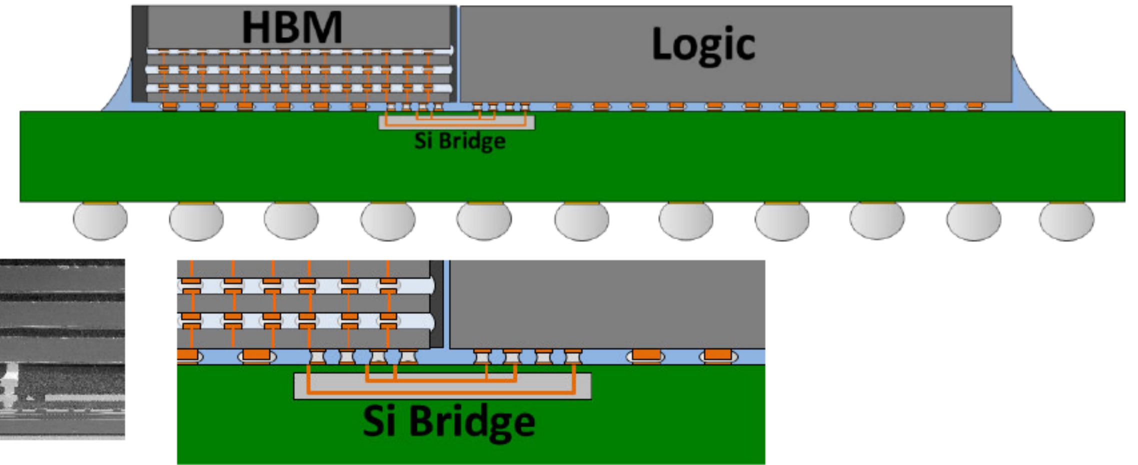


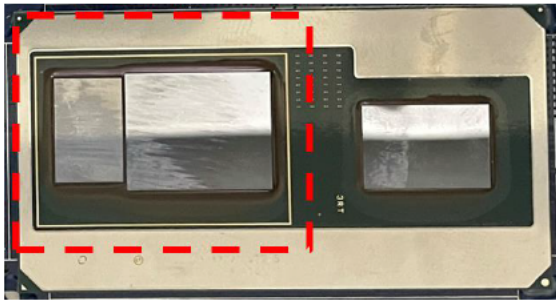


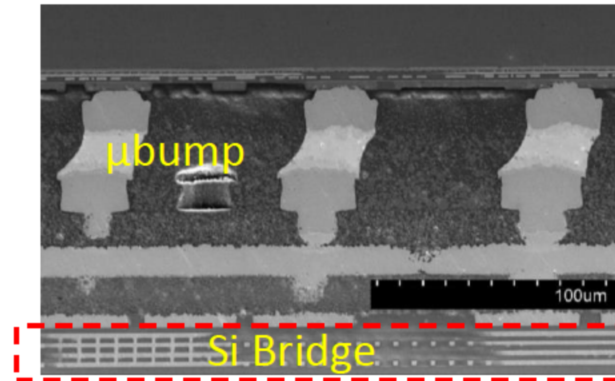
Intel Data Center Max 1550 – 4xHBM, 12x Cache, 8x ‘Xe Memory Fabric’, 16x compute tile, 4x ‘Xe Link Extension’, 2x I/O tile

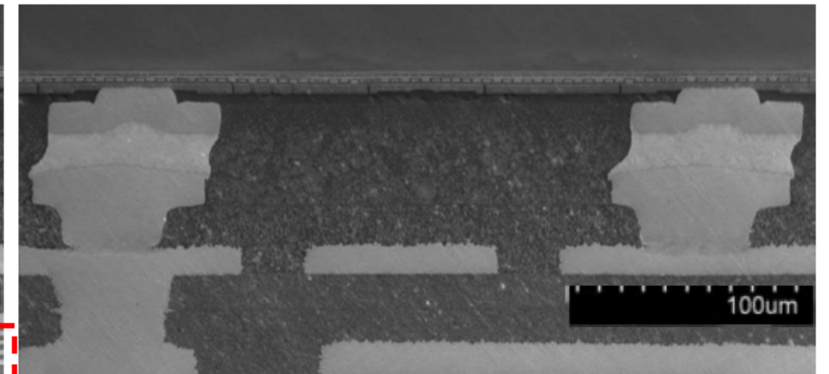
Also used in low-end consumer products

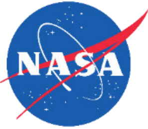
- i7-8705G
  - EMIB
  - Intel CPU, AMD GPU, HBM



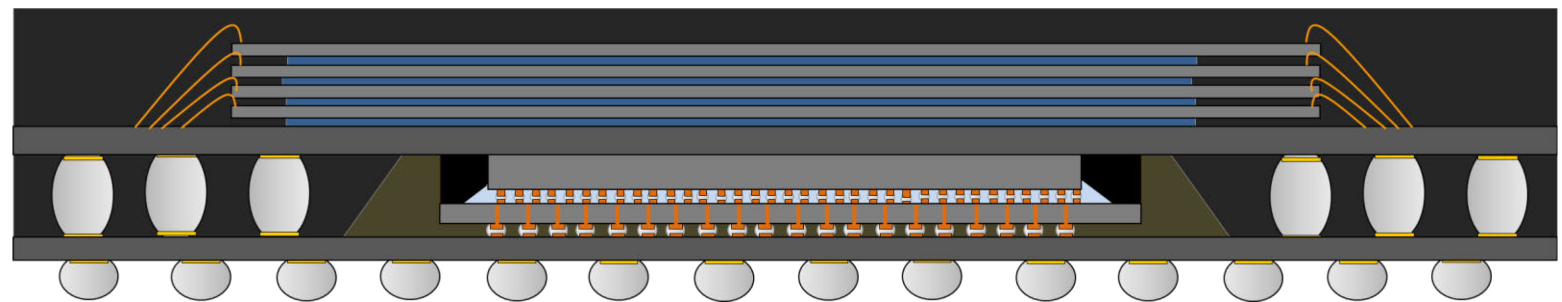


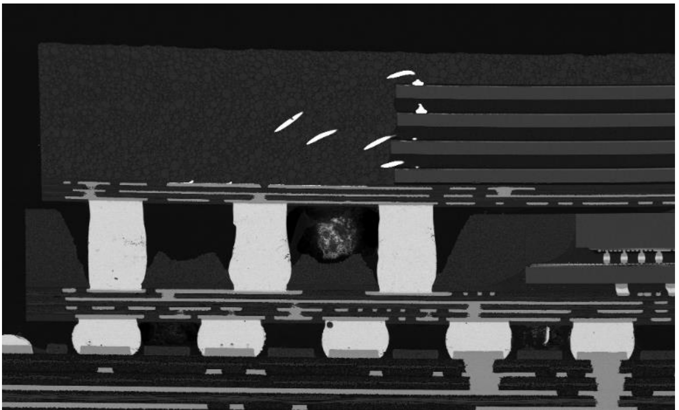


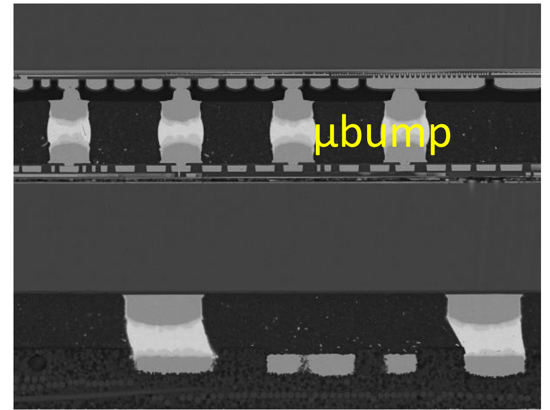




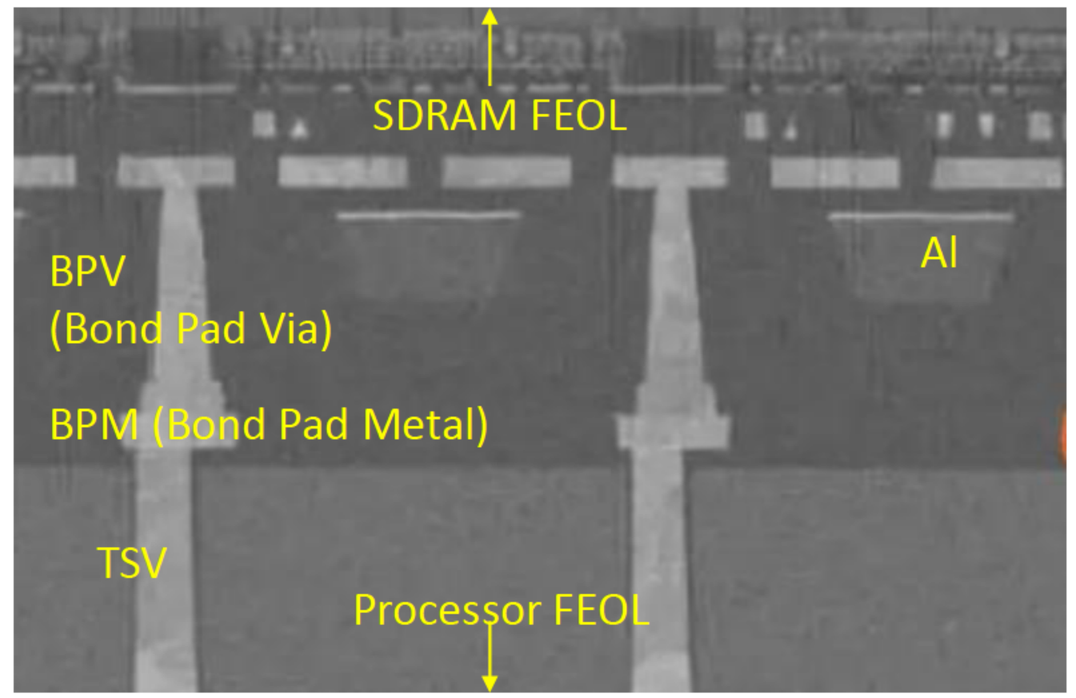
- i5-L16G7
  - Laptop processor
  - Foveros
  - 3D package
  - PoP : Memory above processor



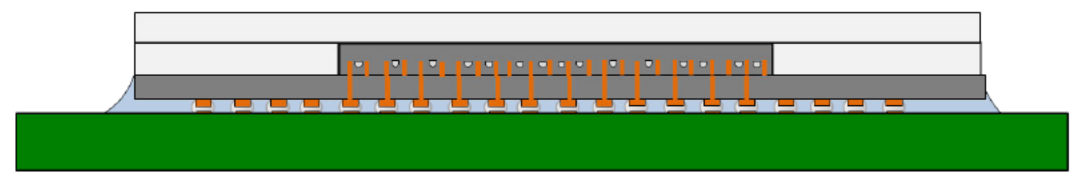


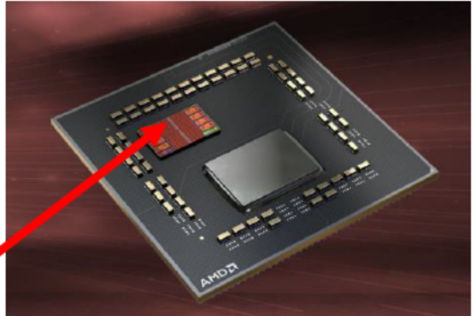


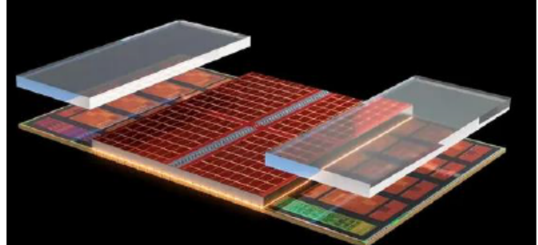
- Ryzen 7 5800 x3D
  - TSMC SoIC
  - Cache memory stacked on processor with hybrid bonding.
  - Al pad embedded in SRAM for wafer testing.
    - Additional back-end process is done after testing.
    - Involves etching away Cu pillar and solder cap formed over the Al pad (US10867929B2).



https://www.amd.com/en/technologies/3d-v-cache

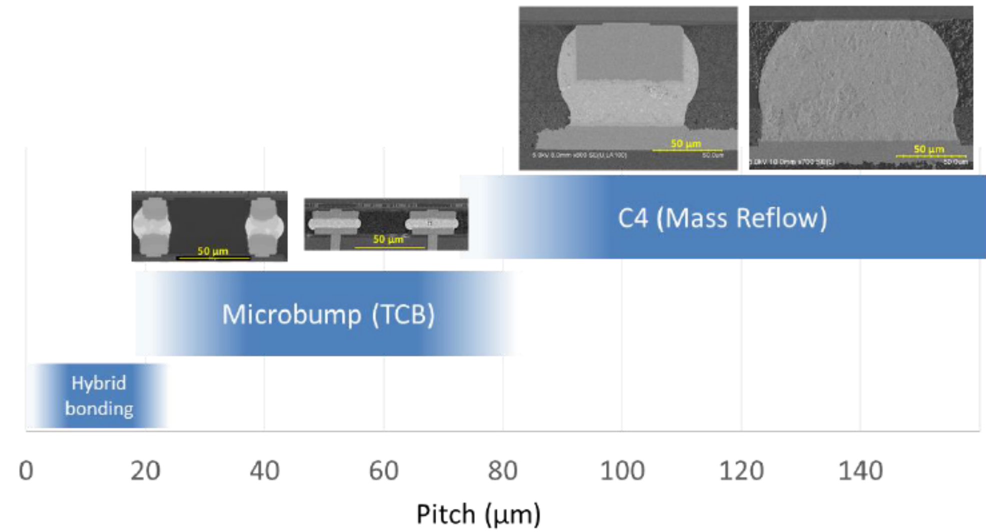


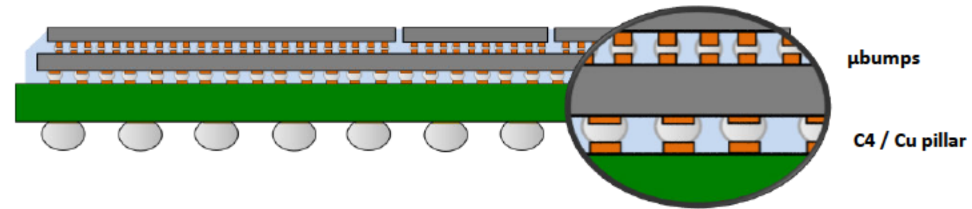


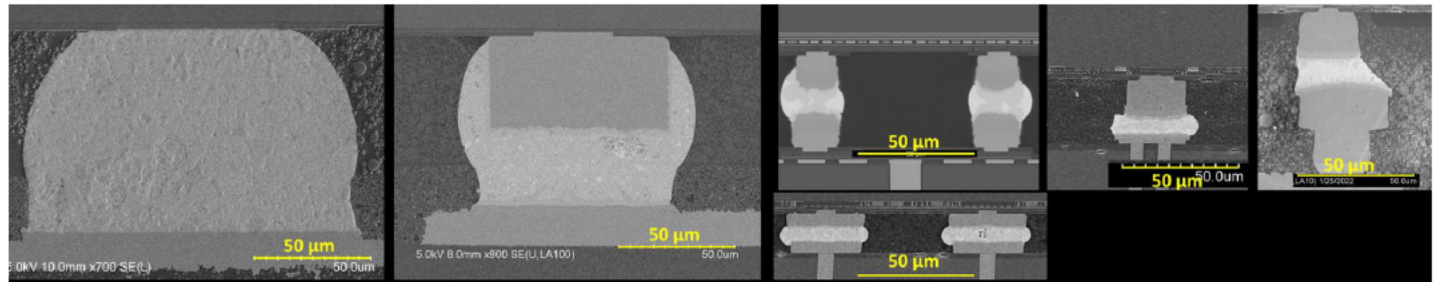


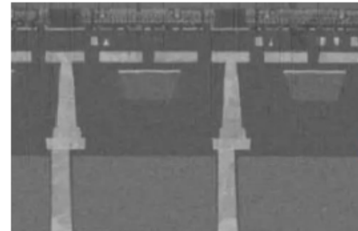
Off-Chip Interconnects : µbump and Hybrid Bonding

- C4
  - Mass reflow (MR)
- µbump
  - Down to ~20µm pitch.
  - Thermocompression bonding (TCB)
- Hybrid bonding
  - Both dielectric and copper are bonded.
  - Wafer-to-Wafer (W2W) or Die-to-Wafer (D2W)
  - D2W is used for HI for yield.
  - High coplanarity is required. No die-to-substrate.
  - Can provide much tighter pitch than µbump
    - D2W: ~9µm in product.
    - W2W: 2.5~8µm, 1µm demonstrated
    - Can be further reduced by sacrificing throughput





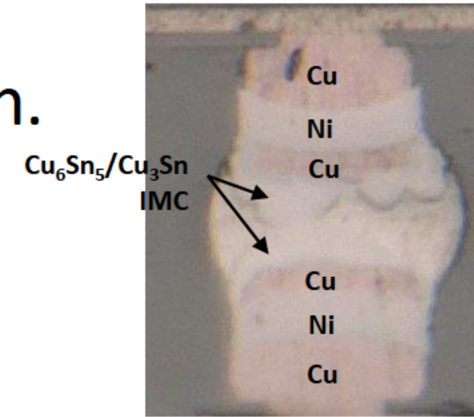


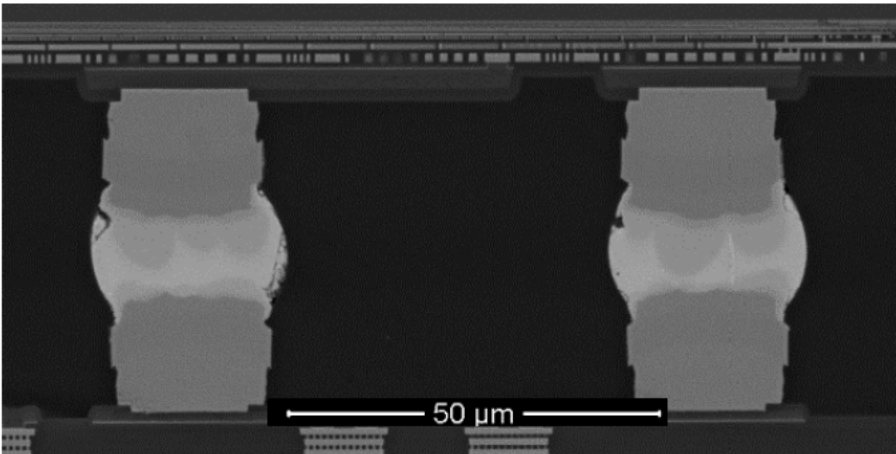


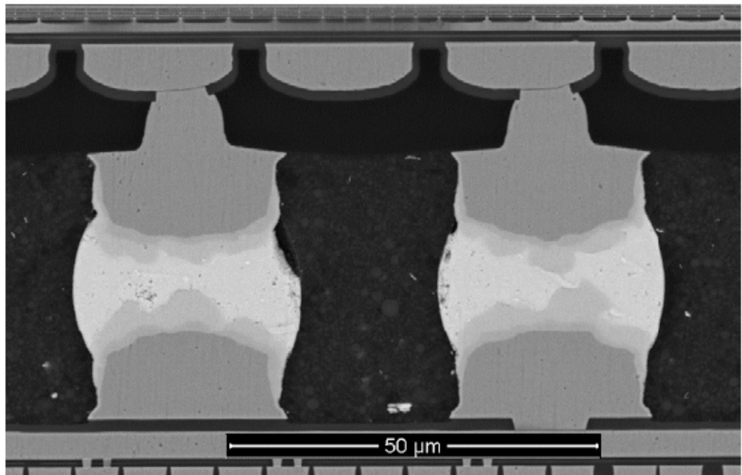
Hybrid bonded memory on CPU

µbump Metallurgy

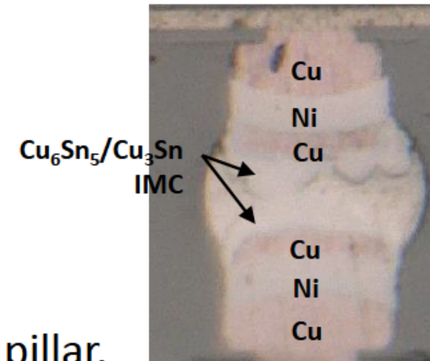
- Many parameter choices exist in µbump configuration.
  - Cu pillar stack up,
  - Solder composition
  - Cu pillar/solder dimension
  - Metallization at upper & lower die, etc
- Parameter interact with each other and affects the reliability.
  - Interfacial reaction : Electromigration, diffusion, IMC growth, Kirkendall voiding
  - Thermal cycling reliability – also depends on stack up
  - Details of impact of µbump metallurgy on reliability is not scope of this talk.



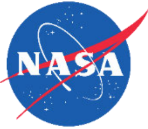




- Principles in C4 are carried over to µbump, with different boundary condition.
  - Less Sn reservoir due to small solder volume.
  - Sn consumption during reflow and thermal aging can change solder composition.
  - IMC-to-solder volume ratio is greater. IMC can dominate overall solder properties. Entire solder can transform into IMC by thermal aging or multiple reflow.
  - Shrinkage voids (≠Kirkendall voids) that does not form in C4 can form, as solder is transformed into IMC.
  - Sn grain orientation starts to play greater role in individual µbump than C4.
- µbumps in most products are typically off-eutectic SnAg.
  - 1.8 ~ 2.5 or 2.8 wt% Ag. (3.5wt% is eutectic)
  - Production : To prevent liquidus temperature becoming too high.
  - Reliability : Ag_3Sn growth control.



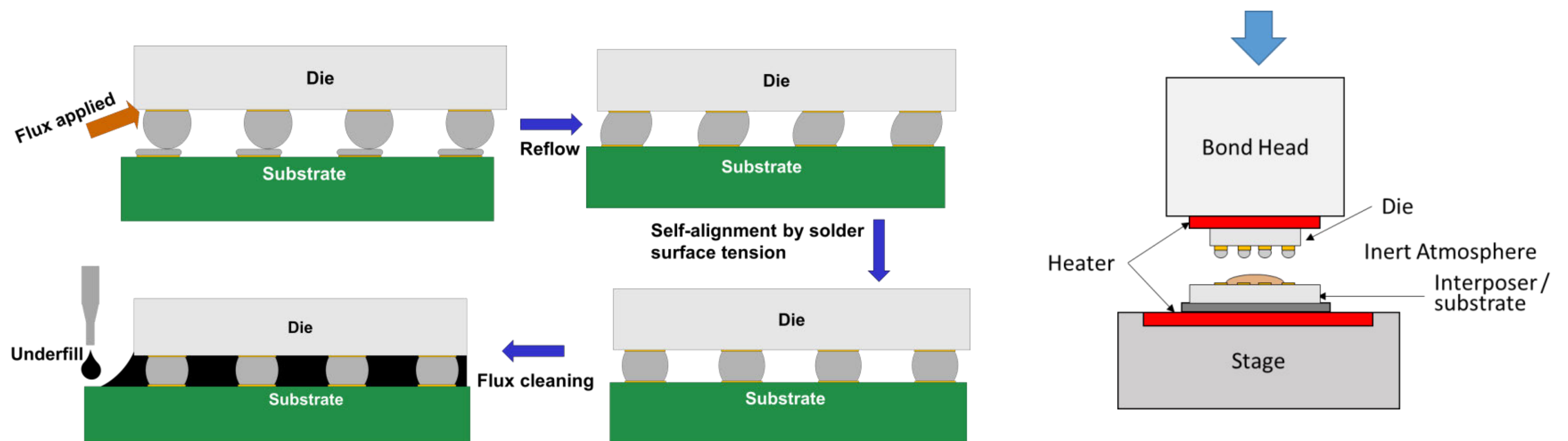
TSMC µbumps typically have Ni barrier in the middle of Cu pillar.

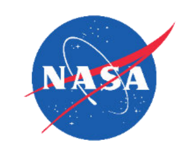


µbump Attach Process

- Mass reflow (MR) is difficult
  - Die placement accuracy : not accurate enough.
    - Need high accuracy due to small solder pitch and volume (no self-alignment).
  - Thinned die : MR cannot easily accommodate thinned die.

    ** Advanced Mass Reflow Molded Underfill (MR-MUF) exists (Hynix HBM3).*
- Thermocompression bonding (TCB)
  - Can accommodate thinned dies. Has greater die placement accuracy (~ ≤2µm).
  - Greater number of process parameters than MR.
    - Stage temperature, bond head time-temperature profile (ramp, contact, peak, release, cool), contact & bond force, bond head displacement, dwell time, etc.
  - Process is done within a few seconds.
  - Different underfill choices : CUF, NCP, NCF

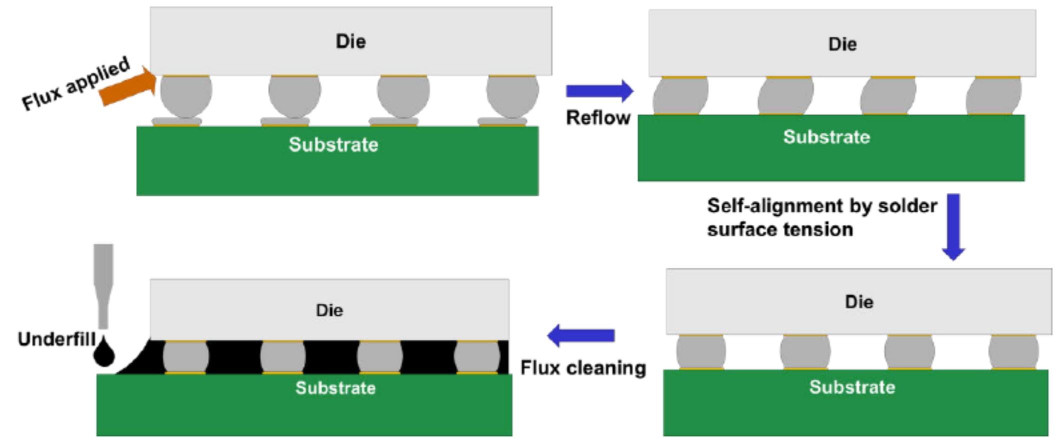


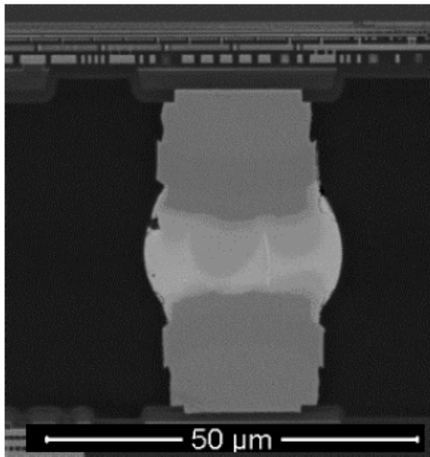


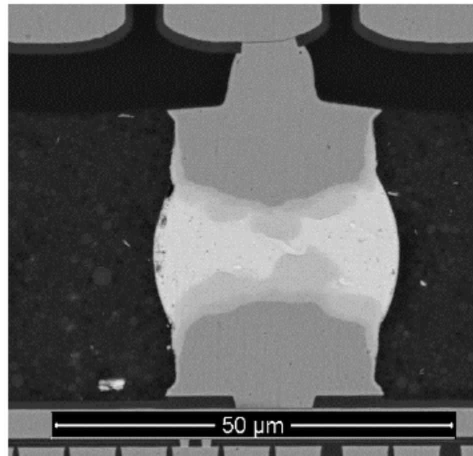
- Post-reflow flux cleaning
  - Tight bump pitch, low height makes flux cleaning very challenging
  - Flux residue around µbumps will cause issues.
    - Corrosion, leakage current, etc.
    - Hinders capillary underfill (CUF) flow.
  - Some use pre-applied underfill to bypass this issue.
    - NCP (non-conductive paste) or NCF (non-conductive film)
    - Have fluxing capability. No flux cleaning is needed.
  - Major companies use multi-step cleaning process different from conventional flip chip process before applying CUF.

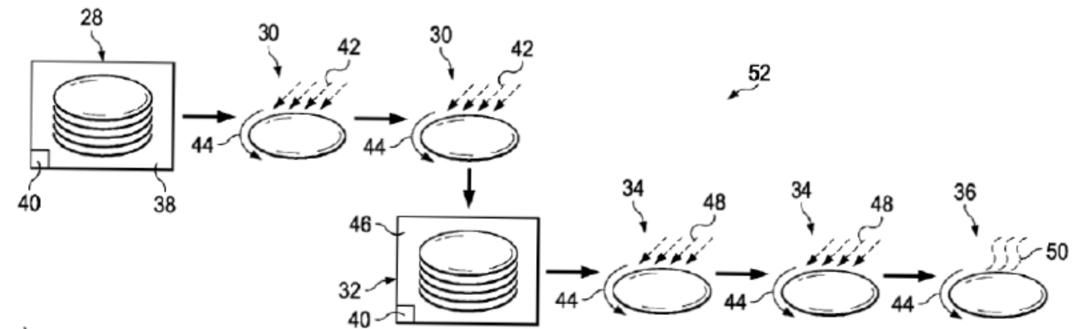
μbump Underfill Process

- CUF
  - The traditional process since C4
  - Flux cleaning and preventing void is the main challenge for large dies with tight pitch bumps.
  - Multi-step cleaning process different from conventional flip chip process.
    - Bath (Softens residue near periphery) → Spray steps (Wash residue away) → Bath → Spray steps → Drying
      - May use ultrasonic or megasonic during bath steps
      - May rotate wafers during spray steps
      - Cleaning solution chemistry also play important role

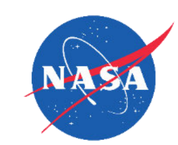






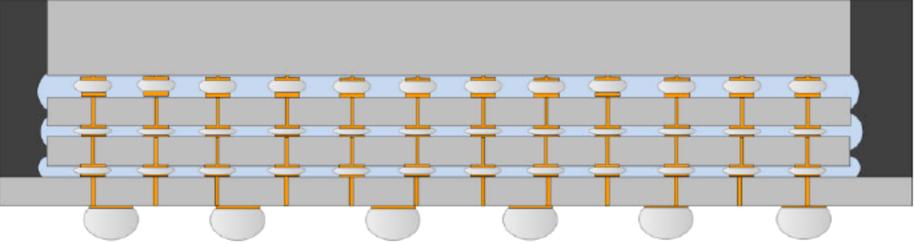


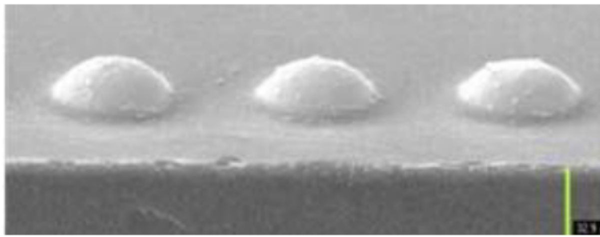
TSMC Patent : US9406500

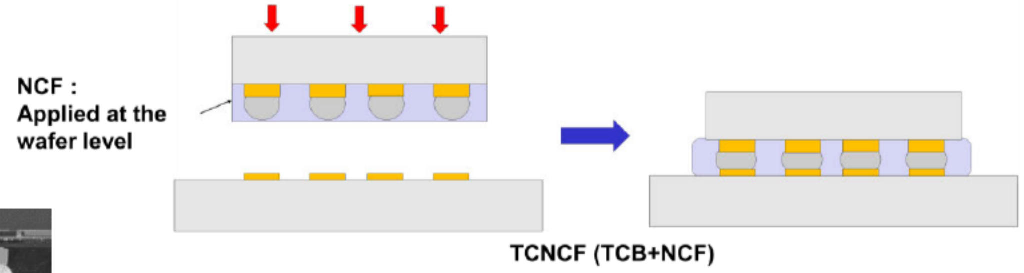


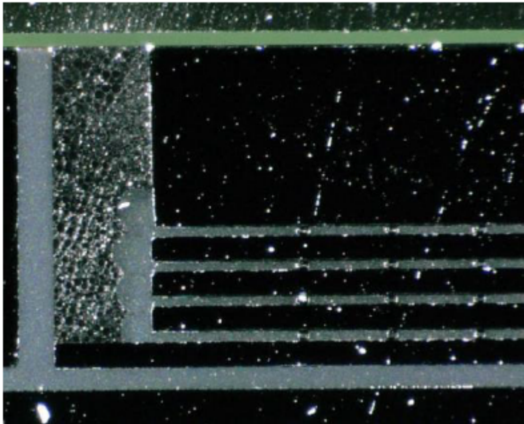
- NCF and NCP
  - Pre-applied
  - Has fluxing capability. No flux cleaning step.
  - Some literatures would even say to use NCF/NCP below ~60µm.
  - Cures within seconds during TCB, unlike CUF.
  - Solder reflow & UF cure takes place simultaneously.
  - Greater force is used during TCB than CUF.
  - Can have defects trapped in the solder.
    - Defect sizes can be below resolution limit of NDE tools. Screening challenges.
  - Most of COTS materials are only compatible with production scale TCB machine with high ramp rate.

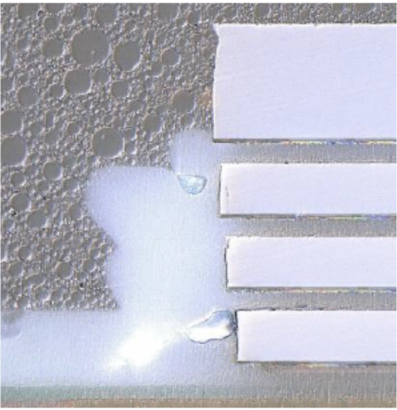
- NCF (non-conductive film)
  - Can be found in most HBMs.
  - Applied at the wafer level. Comes with die.
  - B-stage material.
    - Far greater viscosity than CUF or NC
  - Die will have shelf life.

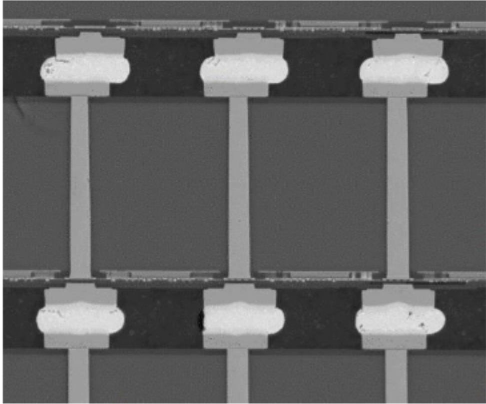


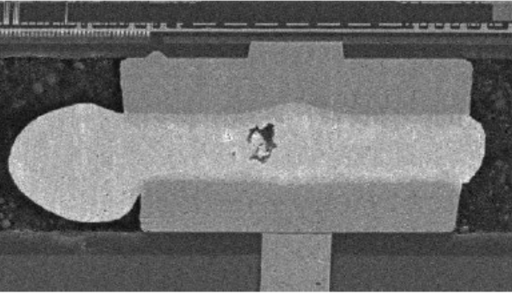


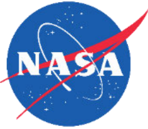




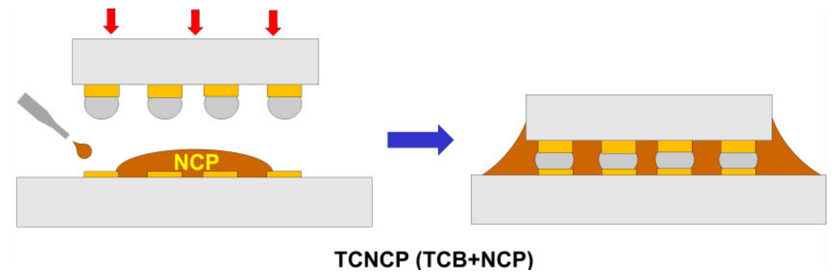


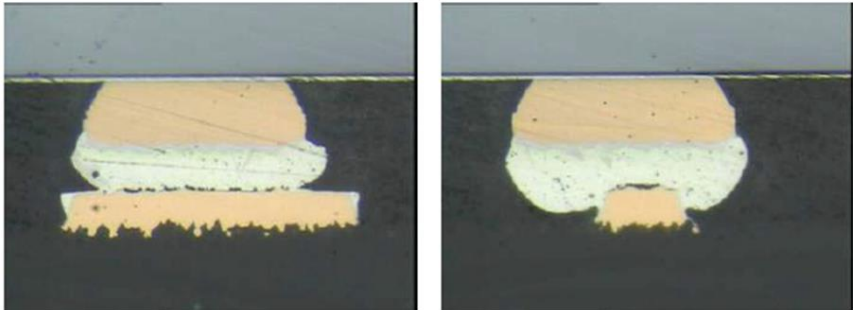




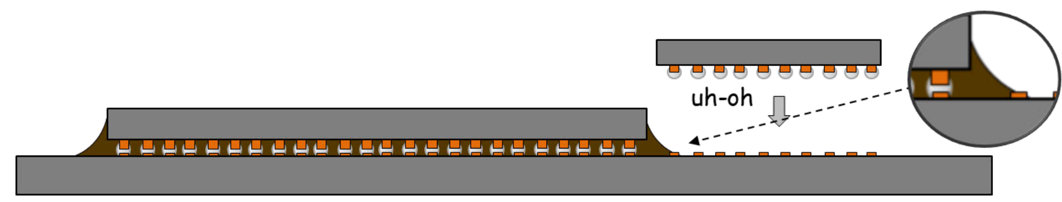


- NCP (non-conductive paste)
  - Applied prior to TCB
  - Need good process control when placing dies close



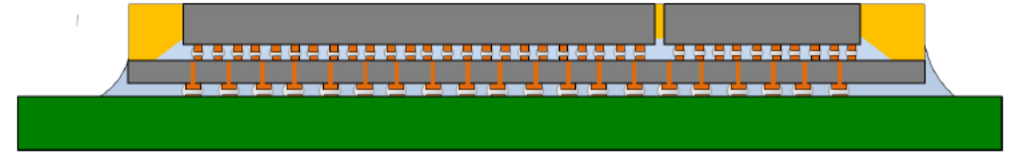


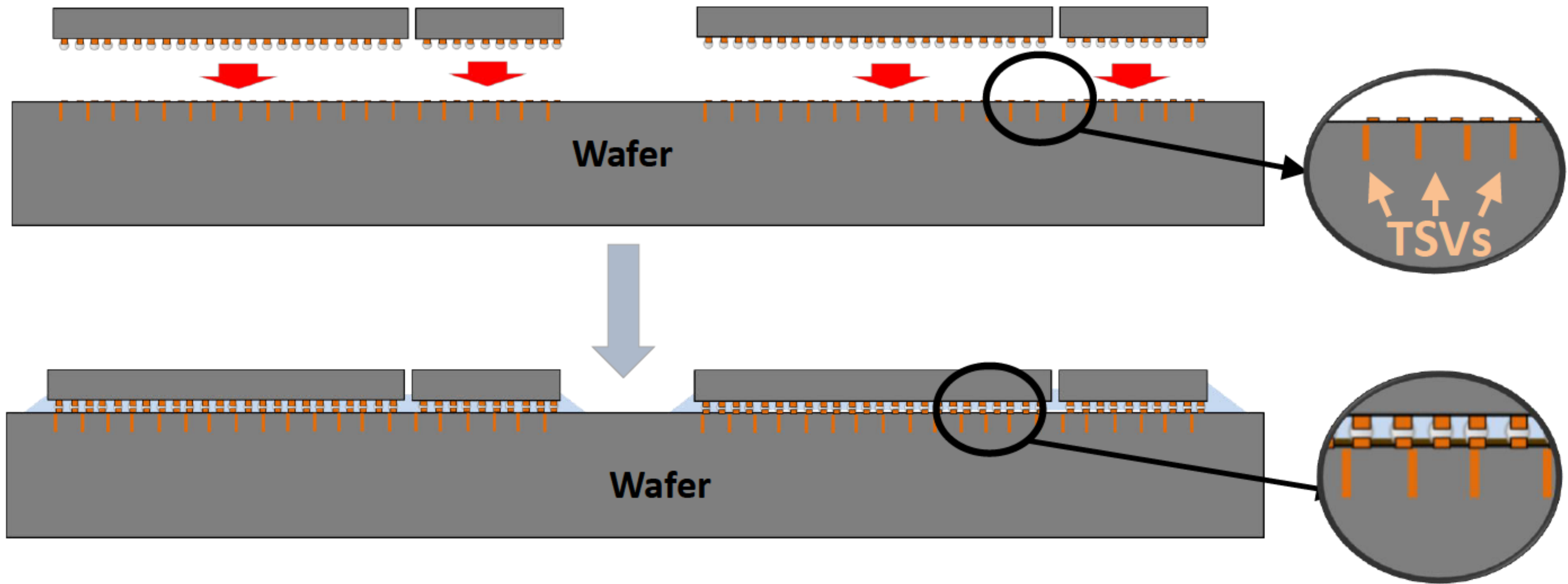
Y.M. Cheung, D Tian, Giuseppe Y. Mak, and Ming Li, EMAP 2013



Typical 2.5/3D Assembly Flow

- TMSC CoWoS-S process is shown here.
  - Intel Foveros uses similar process flow.





1. TCB die attach to wafer
   - Backside of the wafer is not processed yet.
2. Flux cleaning and CUF application

Wafer molding

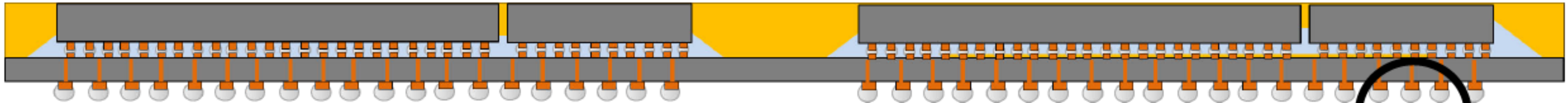
Wafer

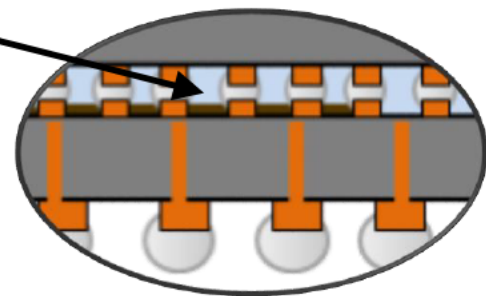
Wafer thinning & backside TSV reveal

** TSMC reported ESD damage of transistors as a "new failure mechanism"*

- *Die pick and place*
  - *Creation of different voltage potential between die and wafer.*
- ***Wafer thinning and back-side TSV reveal** :*
  - *Creation of ESD discharging path between front side transistors and back side TSV surface.*
  - *Potential plasma damage during TSV reveal by recess etching*

C4 Bumping at the wafer backside

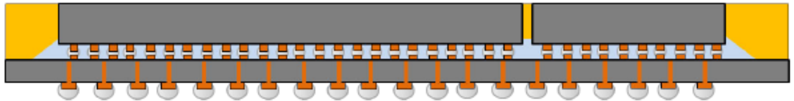


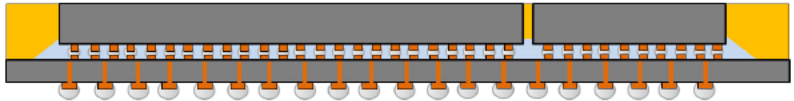


** TSMC also had other issues like open at µbump or TSV/C4 interface.*

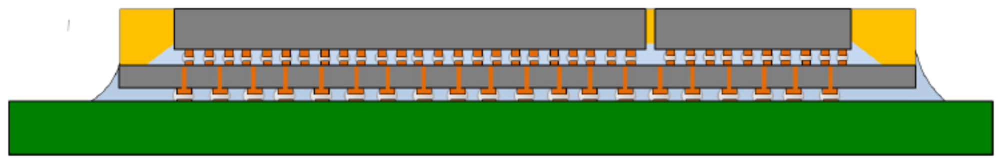
- *Inline inspection/test couldn't catch the defects.*

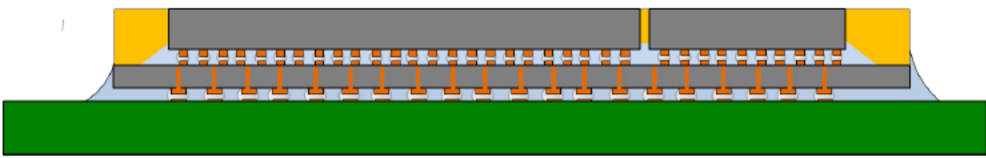
Singulation

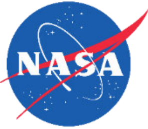




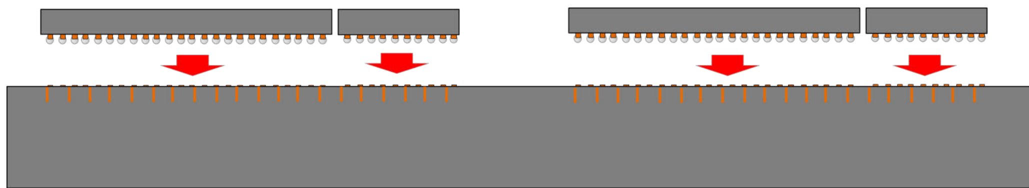
Attach to HDBU substrate

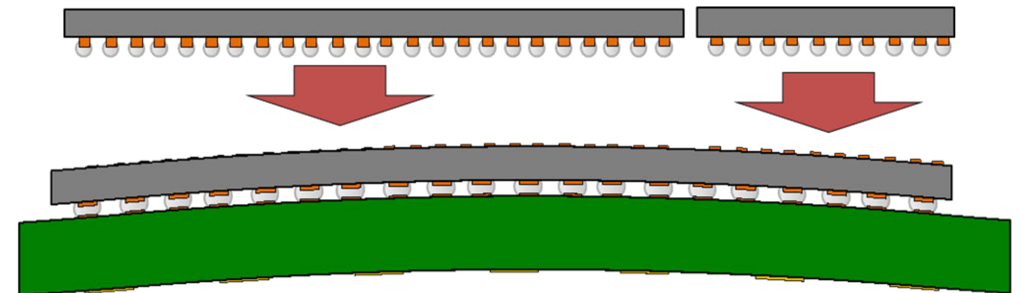


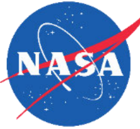




- Why chip on wafer first, like CoWoS-S and Foveros
  - Throughput and yield
  - But also manufacturability
  - If interposer or lower die is already thinned, package assembly can be very challenging.
    - Large + thin = warpage and handling issue
    - Wafer with TSVs with small enough diameter needs to be thinned down.

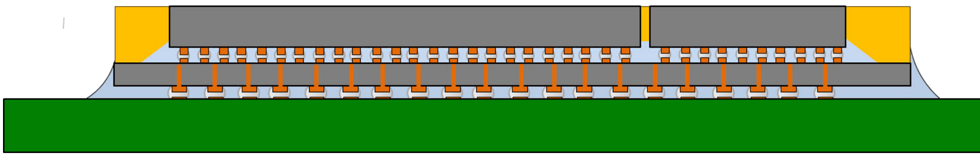


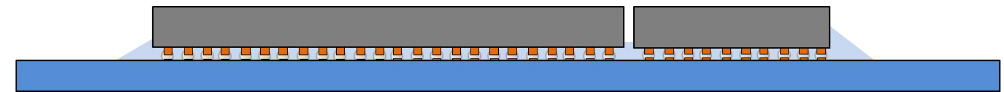


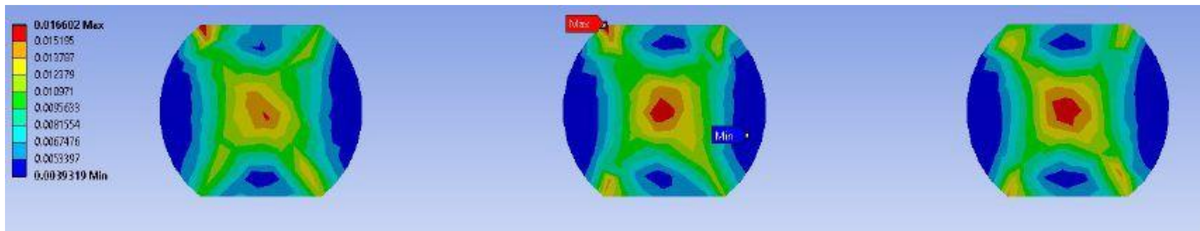


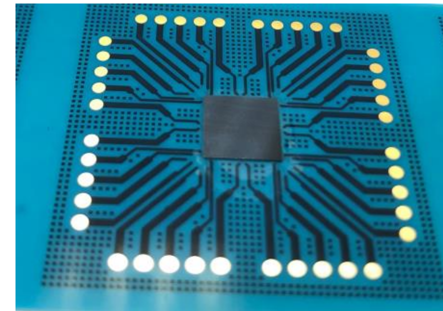
NEPP Study on Glass Core Substrate

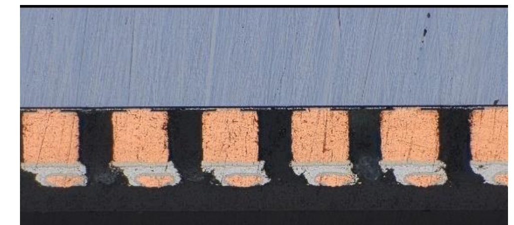
- Glass core substrate can eliminate Si interposer
  - Glass core substrate can provide high line density and small pitch for Advanced Packaging.
  - Intel, Hynix, and Samsung are working on Glass core substrate.



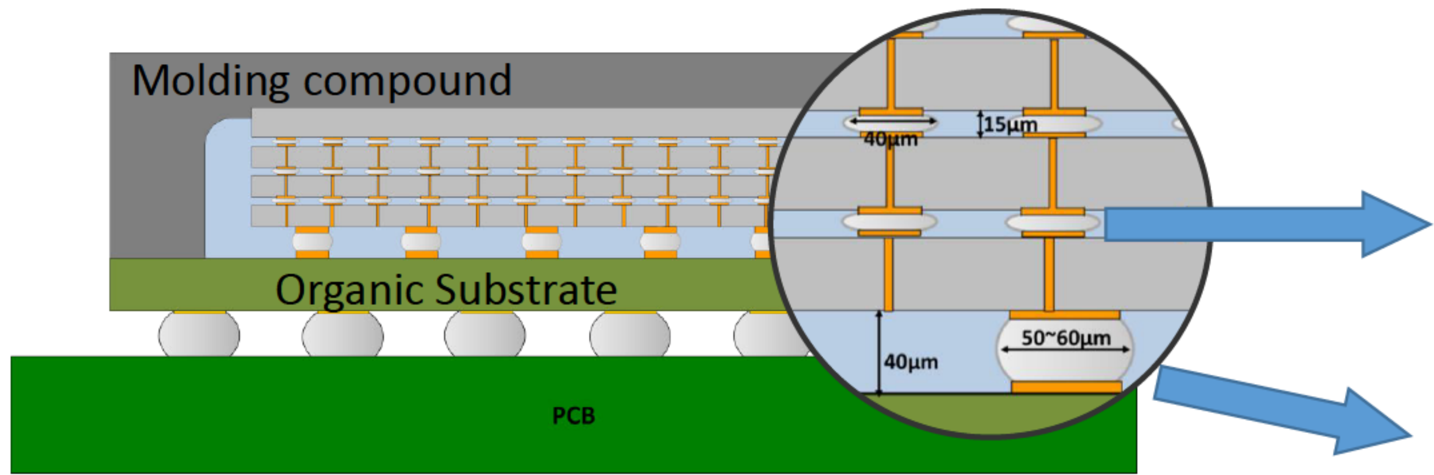




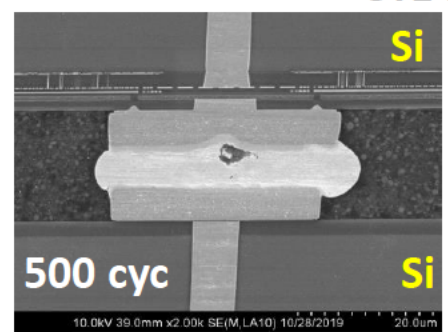


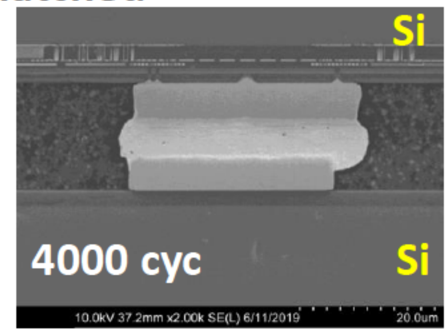


NEPP Study on 3D Memory

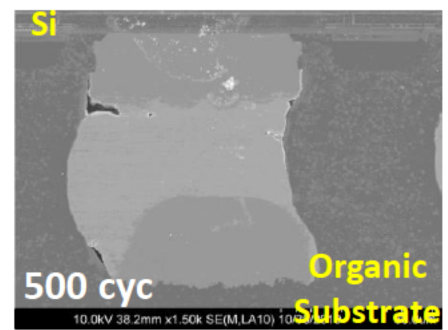


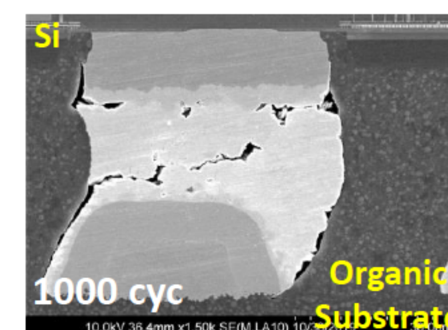
CTE matched





CTE unmatched

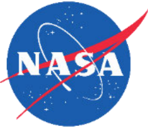




Test type	Mil (mil-prf-35835) Organic Flip Chip	Xilinx FPGA (25x3 units)	Intel FPGA (25x3 or 45x3 units , 1 reject/lot allowed for 45)
Temp cycling	Minimum 150 cyc, Cond B or 100 cyc cond C (*ONLY for underfill, not package reliability: 1000 cyc cond B or C, followed by CSAM inspection of underfill))	1000 cyc, Cond B (JESD22-A113 Preconditioning)	700 cyc Cond B (JESD22-A113 Preconditioning)
High temperature storage	150C 1000 hr	150C 1000 hr	150C 1000 hr (25x3 or 45x3 units , 1 reject/lot allowed for 45)
Biased humidity or HAST	130C/85% 96 hr @bias or 110C/85% 264 hr@bias	85°C, 85% RH, VDD 1,000 hrs or 130°C, 85% RH, VDD, 96 hrs or 110°C, 85% RH, VDD, 264 hrs (JESD22-A113 Preconditioning)	85C 85%RH 1000 hr @Vcc 130C, 85%RH 96 hr @Vcc (JESD22-A113 Preconditioning)
uHAST or Autoclave		121°C/100% RH, 96 hr 85°C/85% RH, 1000 hr 110°C/85% 264 hr 130°C/85% RH 96 hr	121C, 15 PSIG 96 hr 130C, 85% RH 96 hrs

- Mil-PRF-38535 vs commercial FPGA qual condition comparison
  - Commercial qual condition is based on JESD47. 38535 has more tests.
  - MIL-PRF-ATM spec working group in progress
  - Qualification ≠ Reliability
  - APDP is like PIDTP in 38535

JESD22-A113 Preconditioning prior to TC, THB, AC, HAST, uHAST			
Step	Test type	Condition	
1	Initial electrical/visual		
2	Temperature cycling	-40/+60C 5 cyc	
3	Bake	125°C, 24 hr	
4	Moisture soak	MSL3: 192hr 30°C/60%RH MSL4: 96hr 30°C/60%RH	Within 2hr after previous step
5	Reflow	3 reflows	15min to 4hr after previous step
6	Flux immersion	10 sec minimum	Not required for BGA/CGA/LGA
7	Clean & dry		
8	Final electrical		



Summary

- Advanced Packages have very diverse package architectures, manufacturing processes, and materials. They are also evolving constantly and rapidly.
  - The traditional standardized approach used in mil/aerospace component for quality and reliability is not applicable.
- The Mil/Aero spec needs to be agnostic to architecture and manufacturing process flow.
- Making APDP (equivalent to 38535 PIDTP) reviewed by a broader community should be considered.
  - Low-volume OSATs can have many challenges for high-rel due to complex and difficult manufacturing process. Assessing if a manufacture's process is well-established will be far more challenging due to the complexity.
  - There can be also synergistic effects of different stressors and manufacturing defects.
- More tailored approach in defining screening condition may needed.

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