IBM **Semiconductors**

IBM Advanced Packaging in the Northeast Corridor

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IBM Research global footprint

Dublin
Warrington
Zurich
Albany
Yorktown
Cambridge
Almaden
Haifa
Delhi
Tokyo
Shin-Kawasaki
Bangalore
Singapore
Nairobi
Rio de Janeiro
Sao Paulo
Johannesburg

6 Nobel Laureates

10 Medals of Technology

5 National Medals of Science

6 Turing Awards

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3,000
researchers

—

100s
of disciplines

—

Worldwide
collaboration

Artificial Intelligence

Quantum Computing

Semiconductors and Systems

Hybrid Cloud Computing

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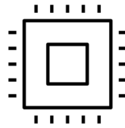
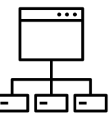
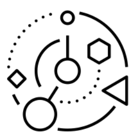
Semiconductors – from smartphones and computers to military assets and national security systems

Logic Technology


Chiplet & Packaging


Design & Enablement on Cloud


Intelligent Fab

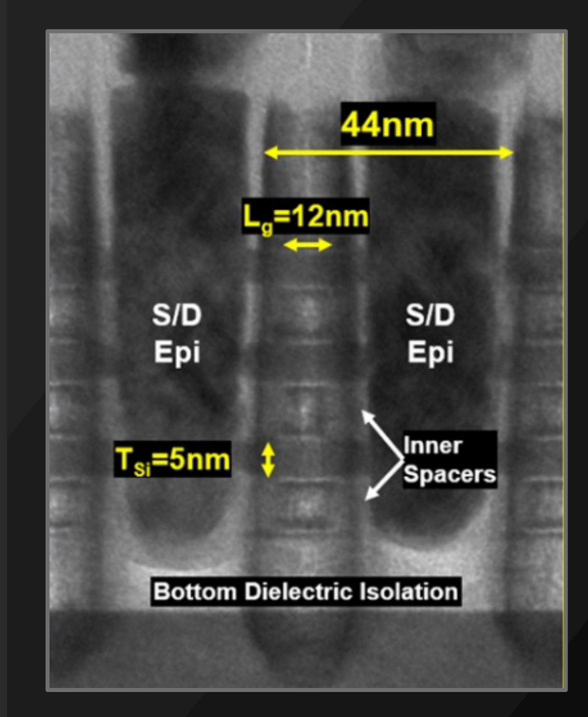
2023 3D Heterogenous Integration
2022 Artificial Intelligence Unit (AIU)
2021 World's First 2-nm Node Chip
2016 Quantum Computing in the Cloud
2012 Atomic Imaging
2011 Watson System
2009 Nanoscale Magnetic Resonance Imaging (MRI)
2008 World's First Petaflop Superconductor
2007 Web-scale Mining
2005 Cell Broadband Engine
2004 Blue Gene/L
2003 5 Stage Carbo Nanotube Ring
2000 Java Performance
1998 Silicon on Insulator (SOI)
1997 Copper Interconnect Wiring
1994 Silicon Germanium (SiGe)
1990 Chemically Amplified
1987 High-Temperature Superconductivity (Nobel Prize)
1986 Scanning Tunneling Microscope (Nobel Prize)
1980 Reduced Instruction Set Computing (RISC)
1979 Thin Film Recording Heads
1973 Winchester Disk Drive
1971 Speech Recognition
1970 Relational Database
1967 Fractals
1966 One-Device Memory Cell
1957 FORTRAN
1956 Random Access Memory Accounting Machine (RAMAC)

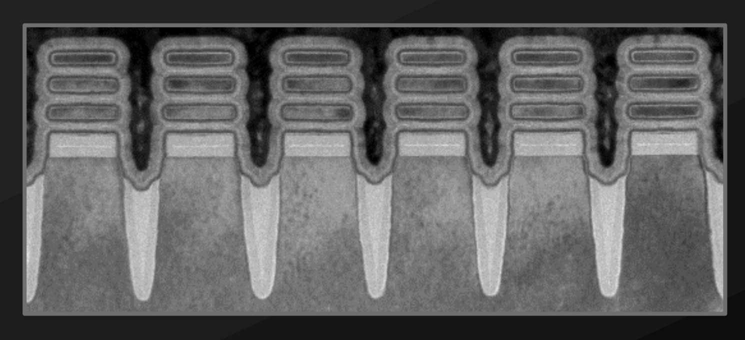
IBM Research produces the world's first 2 nm technology node.

May 6, 2021

45% better performance or

75% less power consumption compared to 7 nm technology.





Big Blue Goes Tiny With World's First 2nm Chip Tech

WIRED

To Make These Chips More Powerful, IBM Is Growing Them Taller

The company reveals a process that it says can cram two-thirds more transistors on a semiconductor, heralding faster and more efficient electronic devices.

IBM Unveils World's First 2 nm Chip

By Sally Ward-Foxton 05.06.2021 3

The New York Times

IBM on Thursday announced another leap in miniaturization, a sign of continued U.S. prowess in the technology race.

Rapidus – IBM Partnership

- Strategic partnership to build advanced semiconductor technology and ecosystem in Japan
- Further develop IBM's 2nm node technology into market-leading offering
- Leverage IBM's long history of successful joint development partnerships in semiconductors
- Rapidus scientists and engineers will work alongside IBM at Albany Nanotech and IBM Japan

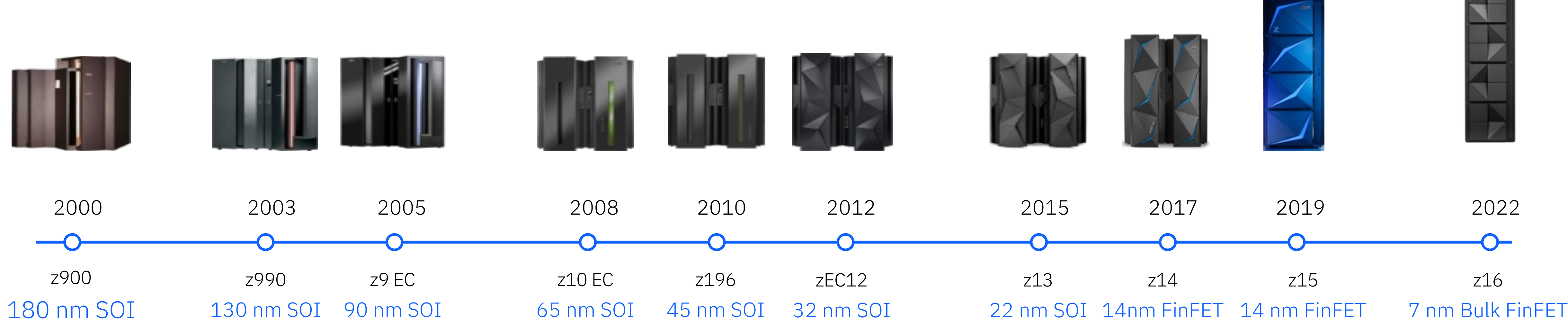
IBM THINK 22 Japan (2nm wafer)

Rapidus Chitose ground-breaking

Rapidus fab rendering

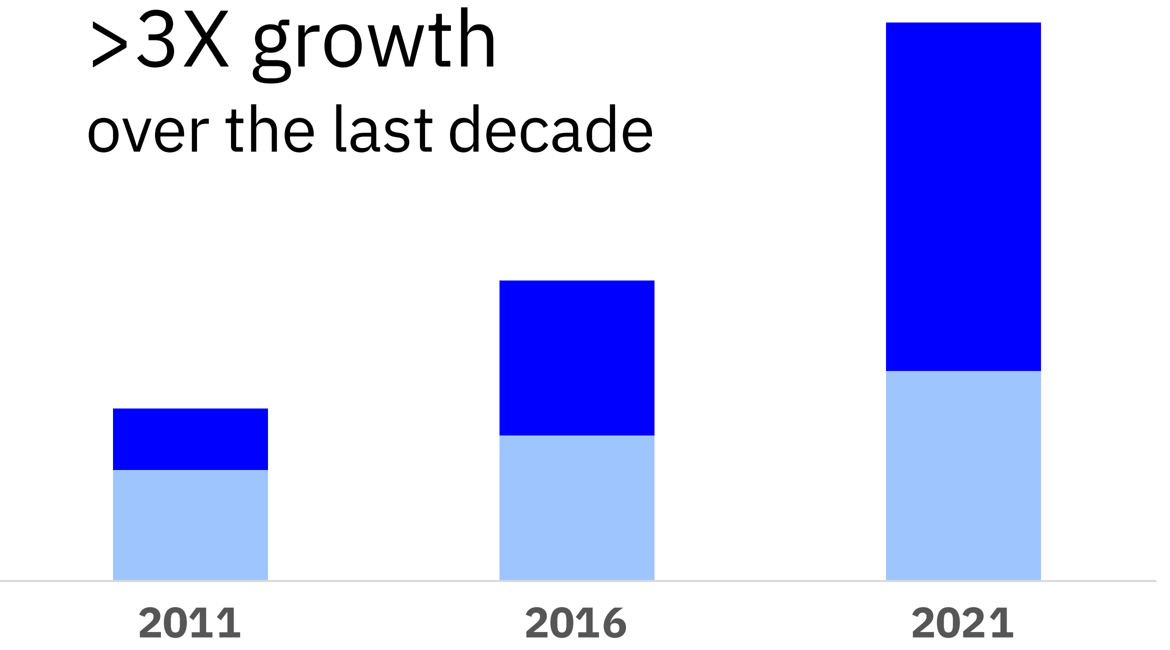
IBM **Semiconductors**

Semiconductor technology is central to IBM's business:
The most reliable, scalable, secure, computing system on the planet.



50+ year history of leading-edge performance and reliability

IBM Z is essential to the world's most critical infrastructure



Workload as measured by installed Million Instructions Per Second (MIPS)

- Classic (CICS, IMS, DB2, Batch) workloads
- New (AI, Linux, Java, C/Python/Go) workloads

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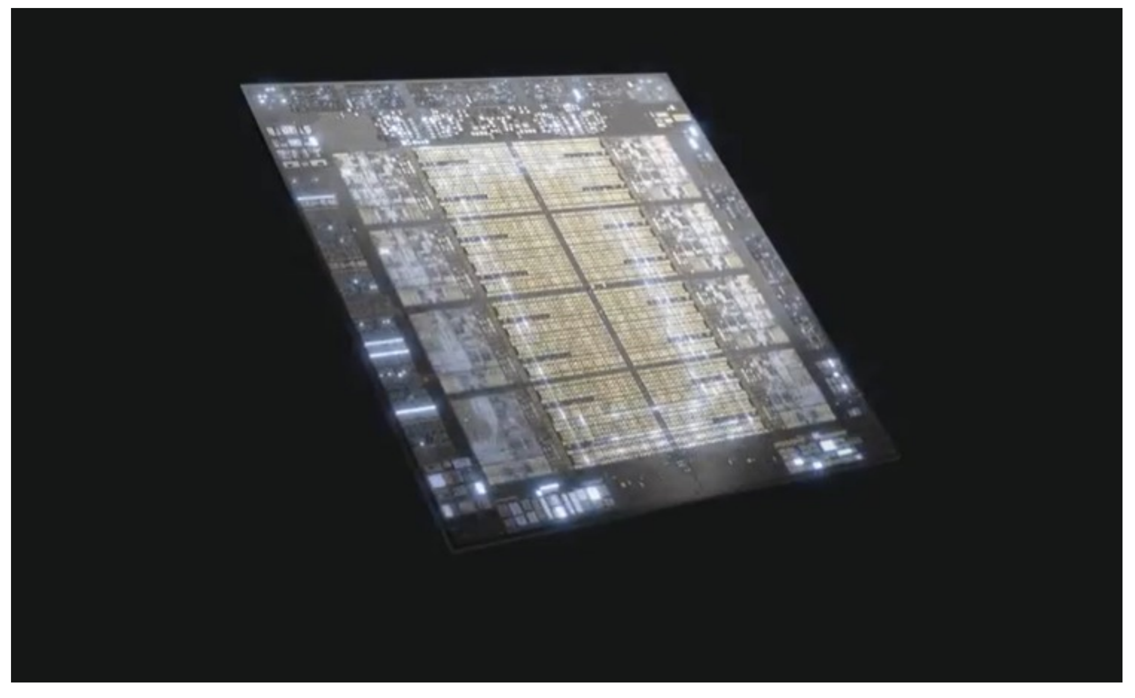
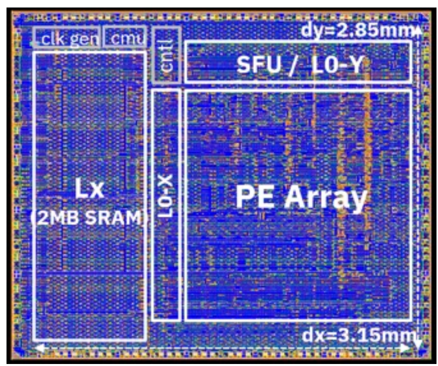
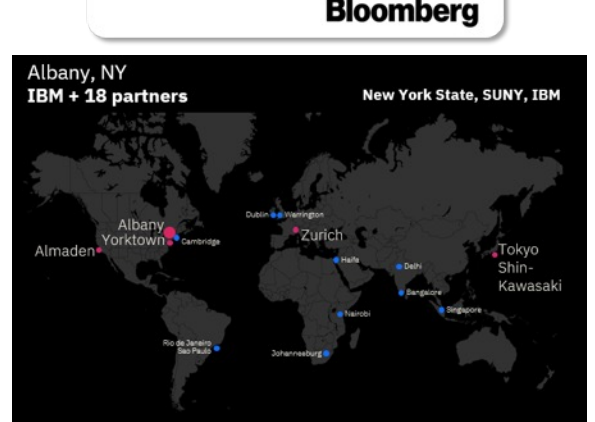
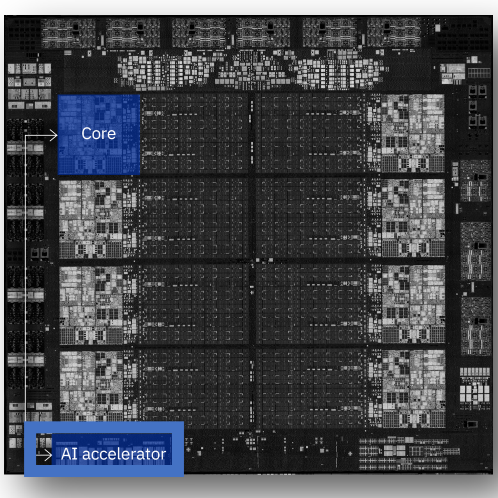
AI Accelerator integration for IBM Z Systems: zAIU



- Focus: Enterprise on-CPU (central processing unit) inference requirements
- AI accelerator (zAIU) integrated into Telum processor
- 8X – 12X overall inference performance
- On-chip AI accelerator enables real-time data inference for applications such as fraud detection

IBM Research AI Hardware Journey

2018	2019	2021	2022
Gen 1 Reduced Precision Core	AI HW Center Launch	AI Core in IBM **Telum** processor	IBM Research Artificial Intelligence Unit (AIU)
			
14nm Technology	Full stack approach	7nm Product	5nm Technology

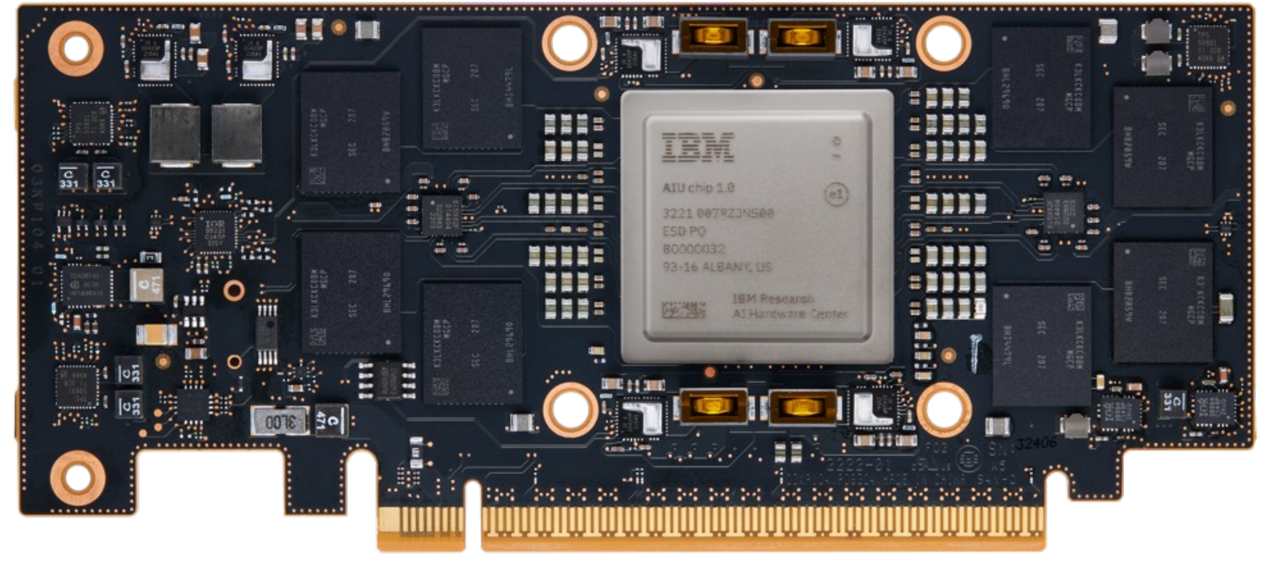
Innovation: computing with less bits

Value: more efficient AI hardware

IBM Research
Artificial Intelligence Unit (AIU)

SoC implements IBM's leadership innovations in low-precision AI arithmetic and algorithms

- Optimized for enterprise AI inferencing and tuning
- Enabled for generative AI
- Supports multi-precision inference (& training)
  - FP16, FP8, INT8, INT4, INT2
- Enabled in the Red Hat software stack
- Runs watsonx.ai
- Implemented in leading edge 5nm technology



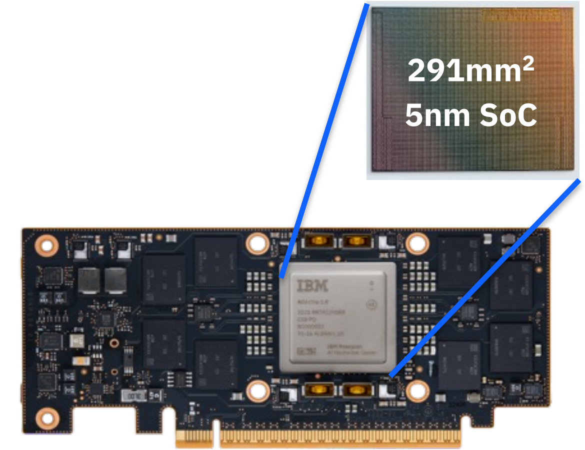
IBM AIU: Packaging Toward the Next AI Accelerators

Key technology enablement:

- State-of-the-art foundry CMOS
- State-of-the-art silicon-verified IP blocks for support functions (memory controllers, I/O interfaces)
- **Chiplets and 3D stacking**

AIU SoC

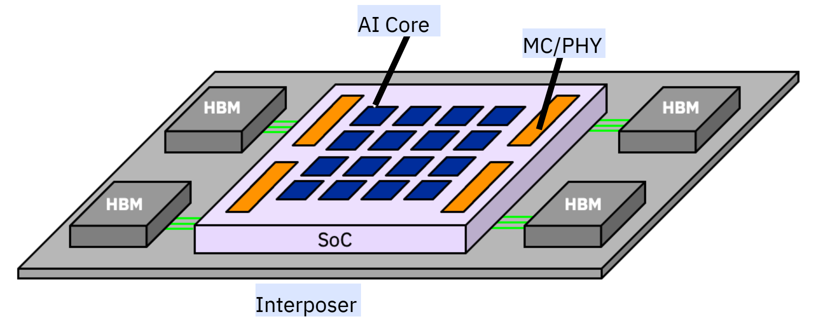
Optimized for FM Inference



2.5D Vision

Optimized for FM Inference, Fine-Tuning, & Training

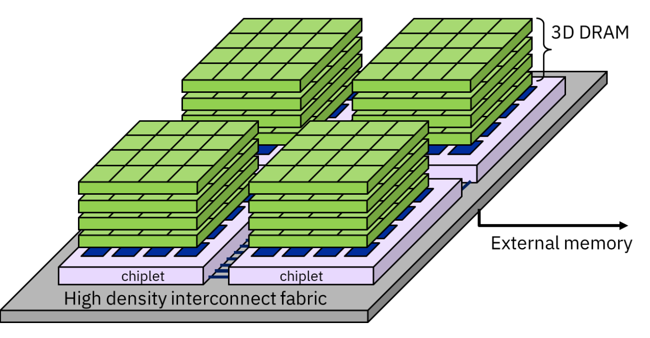
Leverage HBM



3D Vision

Optimized for future very large FM Inference + Fine-Tuning + Training

Leverage 3D-stacked memory + chiplet technologies



Microelectronics Research Laboratory (MRL)

Yorktown Heights, NY

What is the MRL?

- A 200mm wafer-scale unit process development & advanced prototyping facility located in Yorktown
- 50K sf of clean room space, ~200 tools
- Rich history of semiconductor technology innovation (CMP, STI, HiK MG, technology scaling, Cu, SOI, FINFET, Nanowire, SiGe FIN.....)

What makes the MRL unique?

1. Range of capability for advanced prototyping
   - Standard CMOS flow + tools for Packaging and Physical Science applications
2. Flexibility and autonomy
   - Ability and willingness to evaluate new materials while maintaining discipline
   - 193nm & ebeam lithography
3. Breadth and depth of scientific expertise
   - Fundamental understanding of processes
4. Operational discipline
   - Rapid turn-around time
   - Ability to deliver yields

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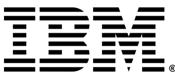
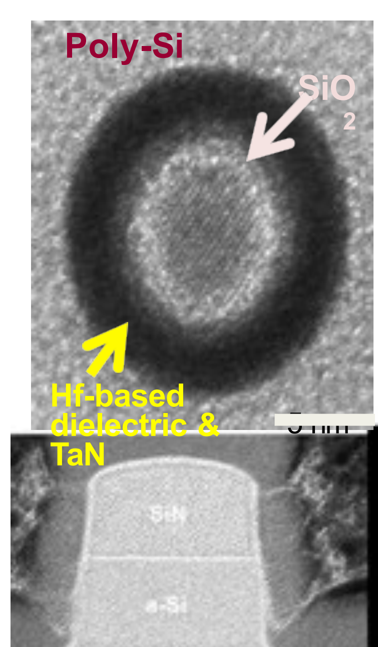
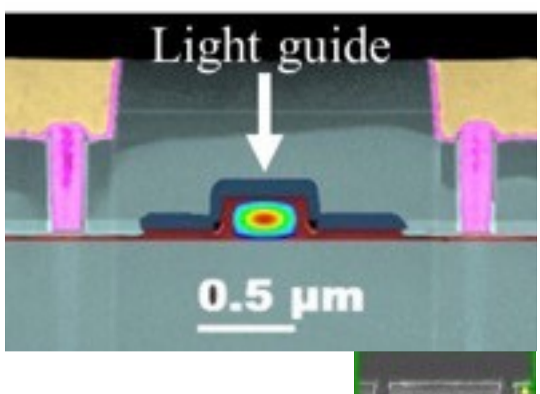


Microelectronics Research Laboratory (MRL)

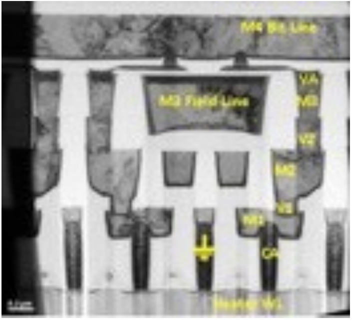
Yorktown Heights, NY

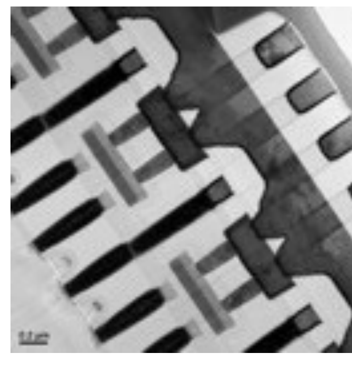


Silicon nanowires, III-V devices

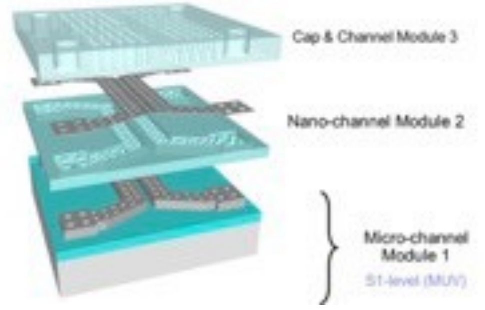


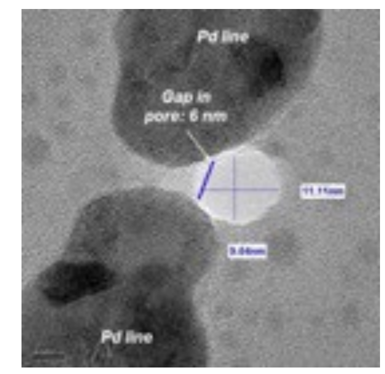
Photonics, 3D integration (TSV)



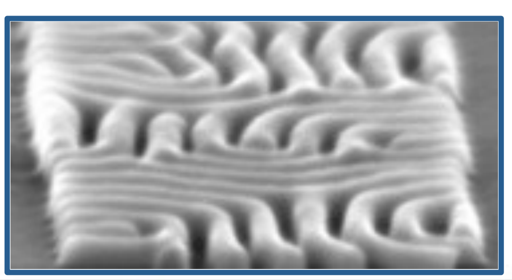


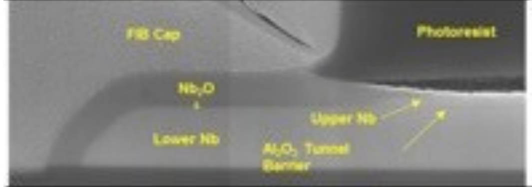
Non-volatile memory (PCM, MRAM)-integration of new materials

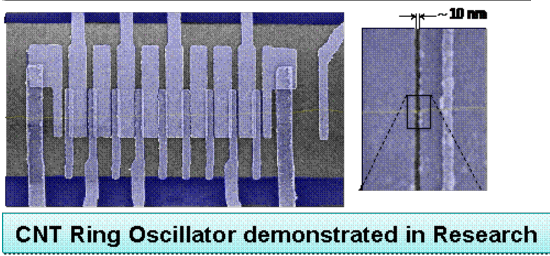




Nanochannel electrodes for sensing biomolecules







CNT Ring Oscillator demonstrated in Research

New devices and nanopattering: Directed self assembly, CNT, QUBIT

MRL offers state of the art processing and the unique opportunity to utilize existing CMOS technology and further integrate novel processes to build nanofabrication capabilities not available anywhere else

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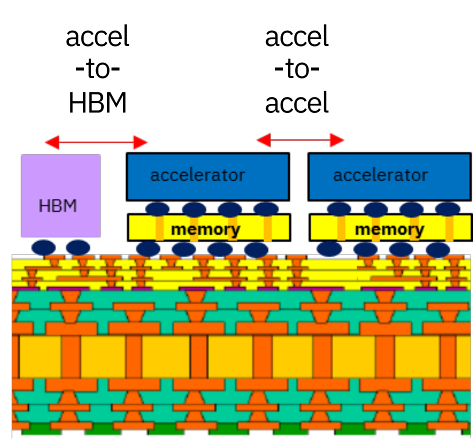
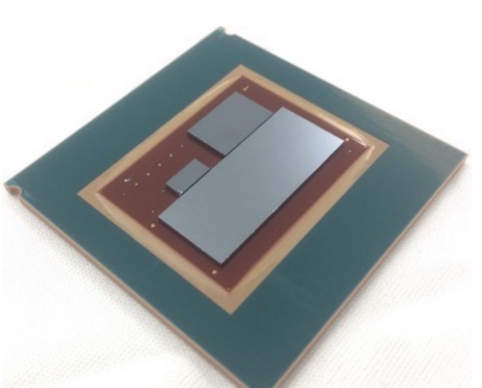
IBM Research Heterogeneous Integration Thrusts

HDI Laminate

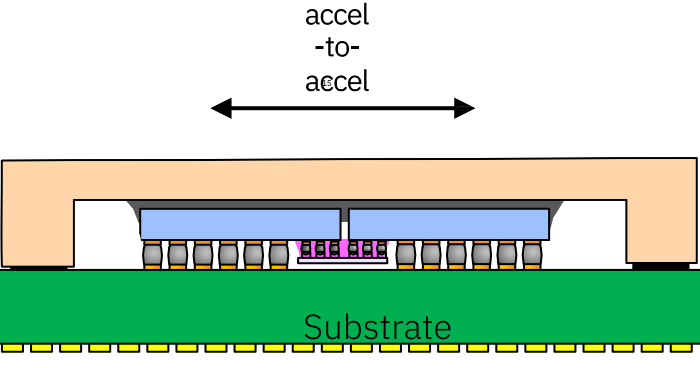
Enables access to tight pitch die interconnects at lower cost

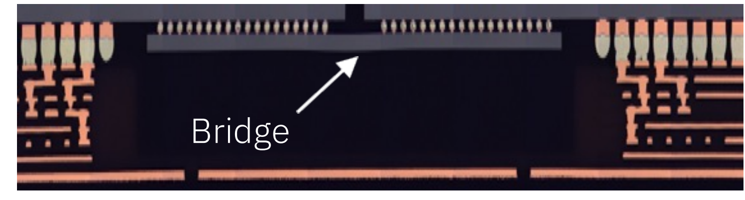




Si Bridge (DBHi)

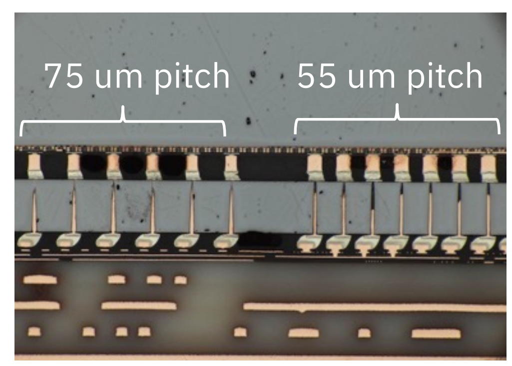
Higher connectivity, flexible configuration

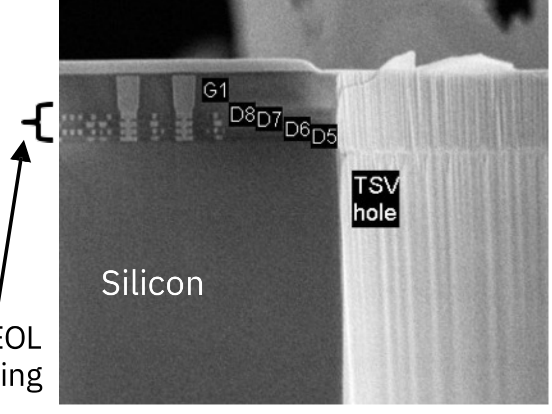




3D Integration

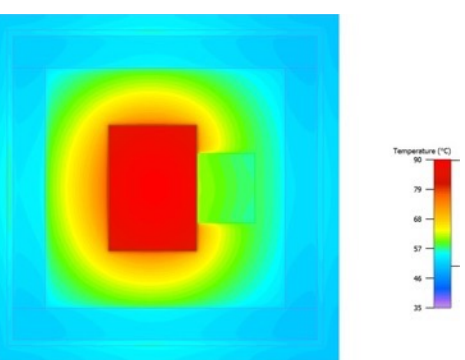
Highest interconnect density, scalable





Simulation & Modeling

SI/PI & wiring analysis, reliability & thermomechanical modeling



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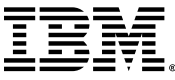
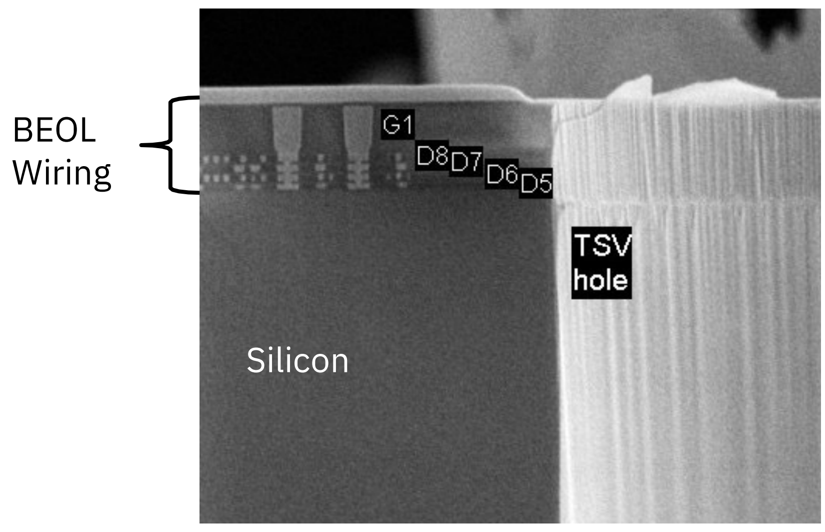
IBM Chiplet Technology Research: 3D Integration

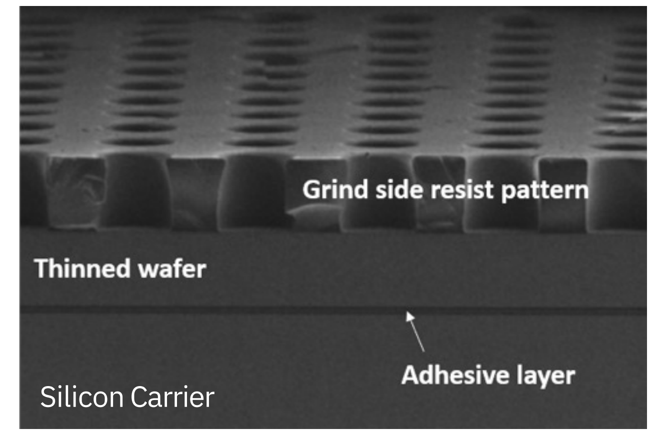


TSV Late Integration



- TSV formation near end of BEOL wiring fabrication
- High current carrying capability
- No impacts to BEOL wiring fabrication
- Need to ensure no BEOL dielectric damage during TSV formation

Wafer Thinning & Backside Process



- Si Carrier with high temp adhesive
- TSV reveal & capture, ensure no Cu diffusion into device wafer
- Laser debond w/ thermally stable release layer – **Industry 1st**
- Reduced warpage
- Enable backside RDL process

Hybrid Bonding

- Die to wafer hybrid bonding
- Inorganic dielectrics
- Advanced dicing technology
- Clean, particle free to ensure no bonding voids
- Cu bonding control & alignment critical

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Semiconductor Research Across Labs

TJ Watson Research Center
- Topological Materials for beyond Cu interconnects
- STT MRAM Materials for mem/storage & exploration of pBits
- Phase Change Matls/RRAM/ECRAM for Analog AI Compute

Tokyo Research Lab
- Materials Innovation for Chiplet Technology
- Jet dispense underfill for Si bridge
- Injection Molded Solder (IMS) bumping technology

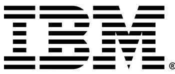
Albany Research Lab
- AI Hardware Center
- Advanced Logic and Packaging

Zurich Research Lab
- Photonic & ferroelectric Materials for Analog AI compute
- Interrogating ferromagnetism at the nano scale
- Thermal effects in nanoscale devices
- Electro-Optical Materials for photonic devices

Almaden Research Lab
- Area selective polymerization for self aligned structures
- MRAM- Atomically engineered thin film deposition capability
- Exploratory materials research at the atomic scale
  E.g. Sensing: Magnetoresistance by spin-polarized tip

IBM Research Albany SI Hardware Center

Albany, NY



$2B
IBM Investment

$300M
New York State Investment

19+
Members of the IBM Research AI Hardware Center

$10B
Total partner investment for High-NA EUV for sub-2nm process development using ASML 5200 system

"IBM: $2B expansion in NY to focus on artificial intelligence"

The Washington Post

Cores and Architecture

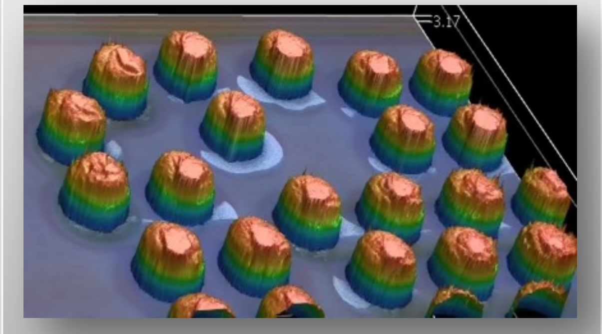
New digital AI cores and architectures, based on fundamental algorithm and computational innovations

Analog Elements

Materials and architectural innovations to enable analog computation for AI inference and training

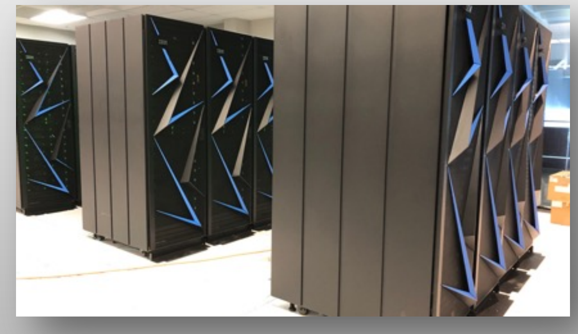
Heterogeneous Integration

Innovations in advanced laminate, Si bridges, and 3D to scale connectivity and mitigate bandwidth bottlenecks



End User AI Testbed

Leverage and develop advanced AI software to utilize new accelerators and capture emerging workload needs



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IBM Research AI Hardware Center Semiconductor Ecosystem

Albany, NY

AI Hardware Center

19+ Members

Advanced Logic and Packaging

SAMSUNG

Ecosystem Partners:

Center for Semiconductor Research (CSR)

IBM Bromont: US DoD Trusted Facility

Bromont, QC, Canada

Canadian government investment in Bromont Canada facility

- MOU with IBM supports large-scale investments in semiconductor advanced packaging
- Joint investment will include increasing capacity and capability including chiplets, 3D packaging, and co-packaged optics

IBM Bromont capabilities

- Supports IBM products including high end systems such as z, Power, and our AIU
- Certified US trusted foundry for packaging of US classified parts
- Capability and capacity to support packaging for other customers

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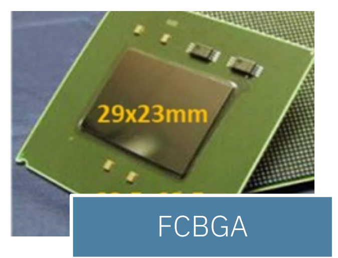
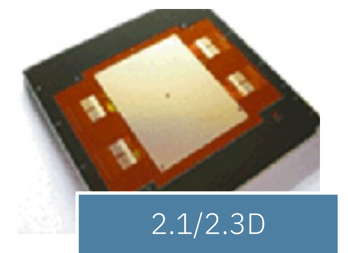
IBM Bromont: Advanced Packaging Examples

Bromont, QC, Canada

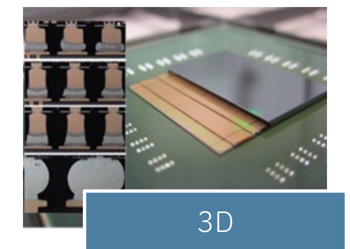


FCBGA

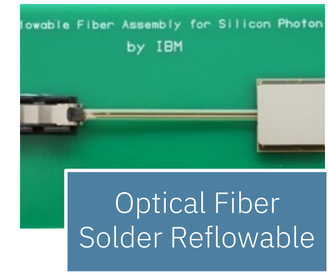


2.1/2.3D

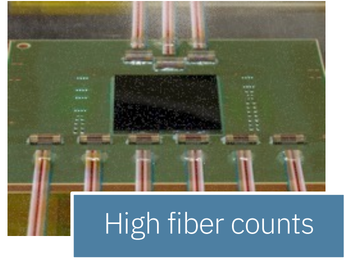
2.5D



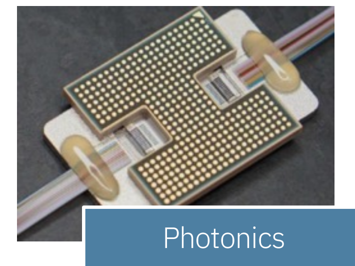
3D



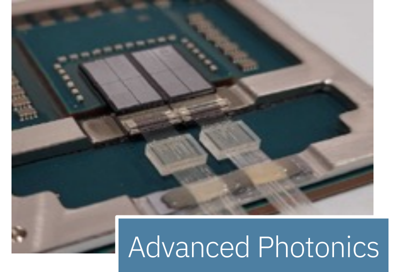
Optical Fiber Solder Reflowable



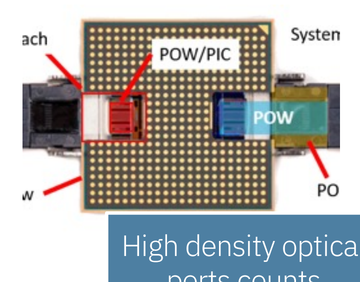
High fiber counts



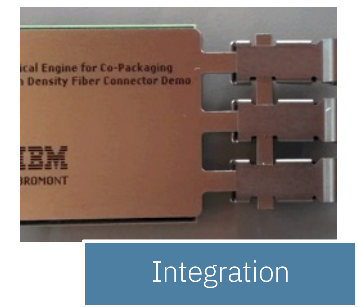
Photonics



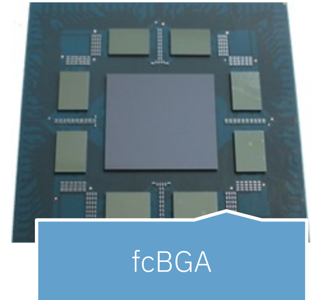
Advanced Photonics



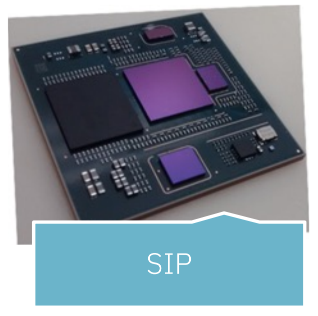
High density optical ports counts



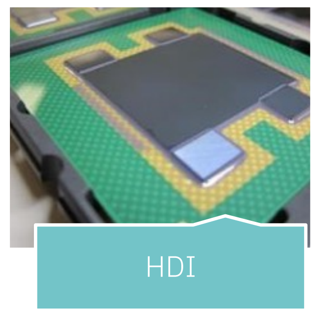
Integration



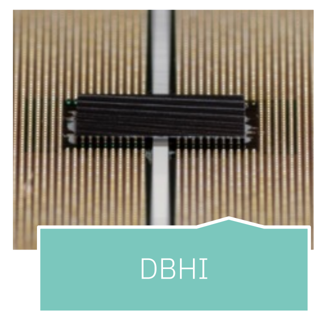
fcBGA



SIP

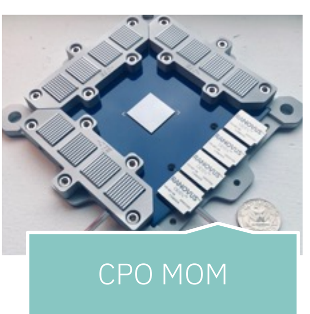


HDI



DBHI

CPO MOM



CPO MOM

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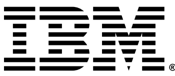
IBM's Advanced Packaging / Chiplet Infrastructure



Watson Research Center – MRL
Broad Research Capabilities

- IBM's Materials Research Lab (MRL) has a long-standing capability in advanced packaging.
- Full process flow capability from materials synthesis all the through assembly and test
- Ability to execute bleeding edge packaging including design and characterization

IBM Albany Research
Wafer-Based HI R&D

- Class 1000 cleanroom space upgraded to support new state of the art HI Line
- Focused on enabling 3DHI technology with hybrid bonding, HD substrate enablement and DBHi bridge technology
- Transfer resulting technologies to IBM Bromont for IBM and OEM use
- Support by TJ Watson for basic research

IBM Bromont / C2MI
Development and HVM

- 50 year of packaging manufacturing experience serving both IBM and external customers (majority) for advanced flip chip, SiP and test production
- Partnered with C2MI technology incubator
- Massive expansion planned in both capability and capacity supported by Canadian Government funding

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Bridging the Valley of Death with Fab-Scale Research

Required Investment

IBM Microelectronics Research

- Provides access to scale early-stage prototyping
- Connects researchers with fabs to facilitate transition
- Offers repeatable processes, back-end manufacturing / integration and full flow-fabrication

Flexibility & Autonomy
Ability and willingness to evaluate new materials

Operational Discipline
Rapid turn-around time; ability to deliver yields

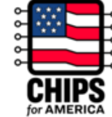
200MM Wafer-scale unit process development & advanced prototyping facility

Lab to Fab Transition
Evaluation at 200mm wafer scale for transfer into 300mm

Proof of Concept → Lab Prototyping → Foundry Prototyping → Capacity Production → Demonstration of Production Rates → DOD & Commercial Adoption

Valley of Death

Government Engagement & Activity



Microelectronics Commons

NORDTECH
Northeast Regional Defense Technology Hub

Northeast Regional Defense Technology (NORDTECH) Hub

Hubs

DEPARTMENT OF DEFENSE
Air Force Materiel Command (AFML)
Air Force Research Lab (ARL)
Army Contracting Command (ACC)
Army Research Lab (ARL)
Army Research Office (ARO)
DARPA
Naval Information Warfare Center (NIWC)
Office of Naval Research (ONR)

INTELLIGENCE COMMUNITY

DEPARTMENT OF ENERGY
ARPA-E

FEDERAL LABS
Brookhaven National Lab
Lawrence Livermore National Laboratory

OTHER
National Institute of Health (NIH)
National Science Foundation (NSF)
US Agency for International Development (USAID)

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Leveraging Existing Regional Facilities

NORDTECH
Northeast Regional Defense Technology Hub

SkyWater
Minneapolis, MN

Griffiss Institute
Rome, NY

NY CREATES & AIM Photonics
Rochester, NY

Cornell NanoScale Science and Technology Facility (CNF)
Ithaca, NY

IBM Research
Yorktown Heights, NY

GlobalFoundries
Malta, NY

GE Research
Albany, NY

Rensselaer Polytechnic Institute
Troy, NY

Albany NanoTech Complex:
- NY CREATES
- AIM Photonics
- University at Albany College of Nanotechnology, Science & Engineering
- IBM Semiconductor

Albany, NY

IBM Bromont
Bromont, Quebec

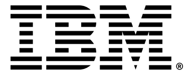
GlobalFoundries
Burlington, VT

Brookhaven National Lab
Upton, NY

NYU Center for Cybersecurity & Nanofabrication Facility
Brooklyn, NY

Prototyping Facility
Core Facilities

RAMP-C



Rapid Assured Microelectronics Prototypes - Commercial

U.S.-based fabrication of leading-edge custom integrated circuits and commercial products for critical DoD systems

- Phase 1: Complete
- Phase 2: Performing
- Phase 3: To-be Awarded

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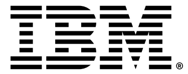
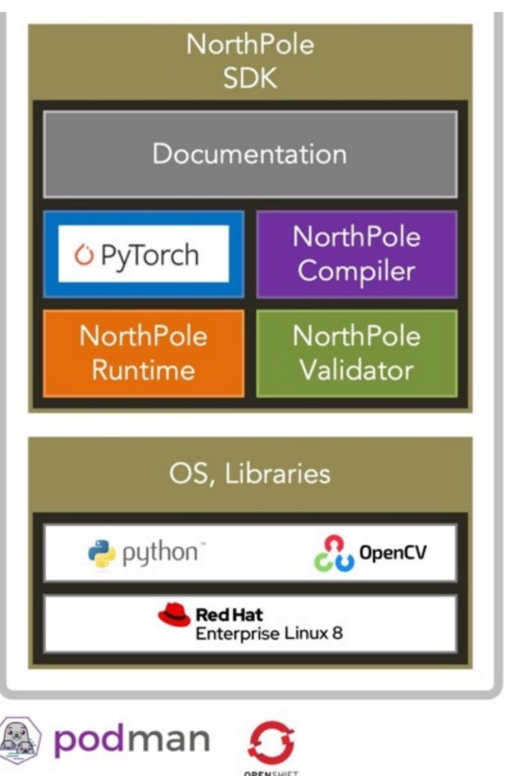
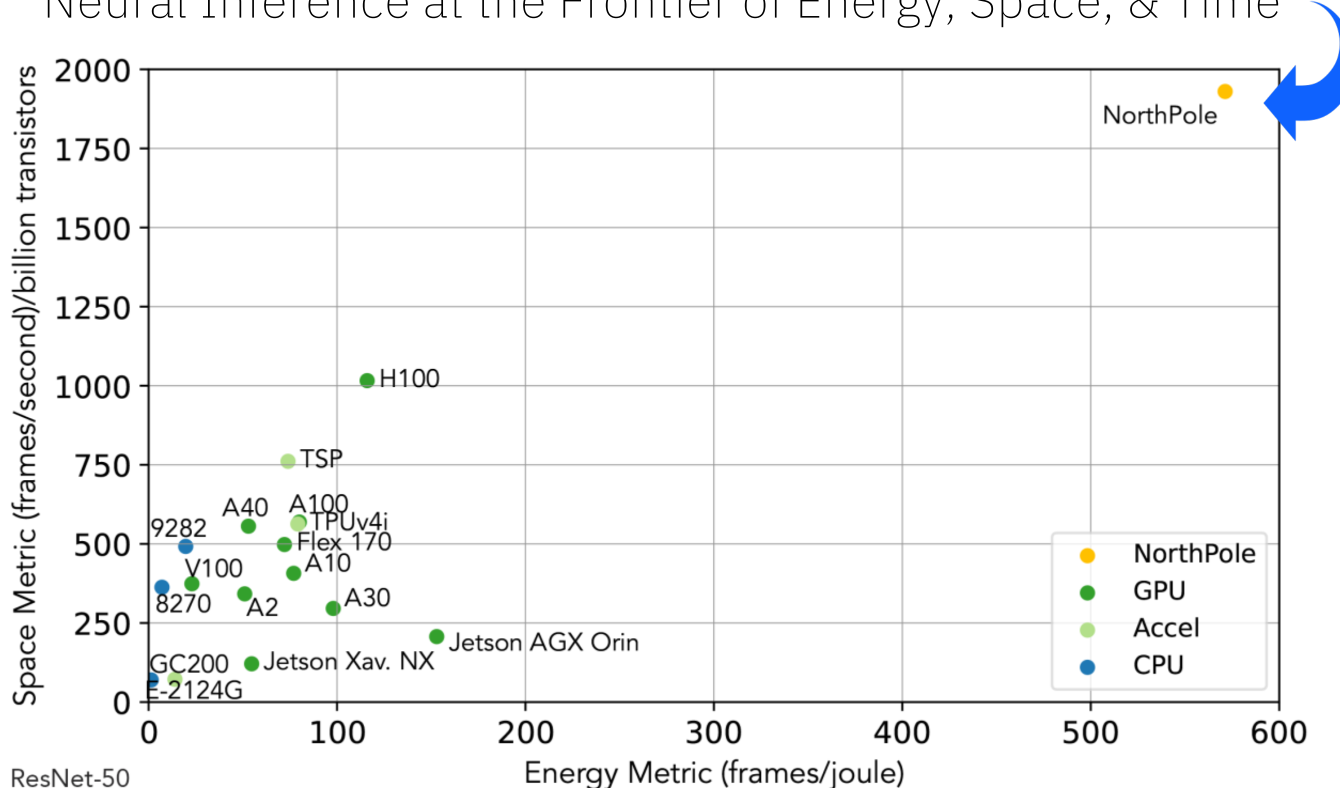
Northpole



Brain-inspired computer chip that can supercharge AI by working faster with much less power

NorthPole has an end-to-end containerized toolchain





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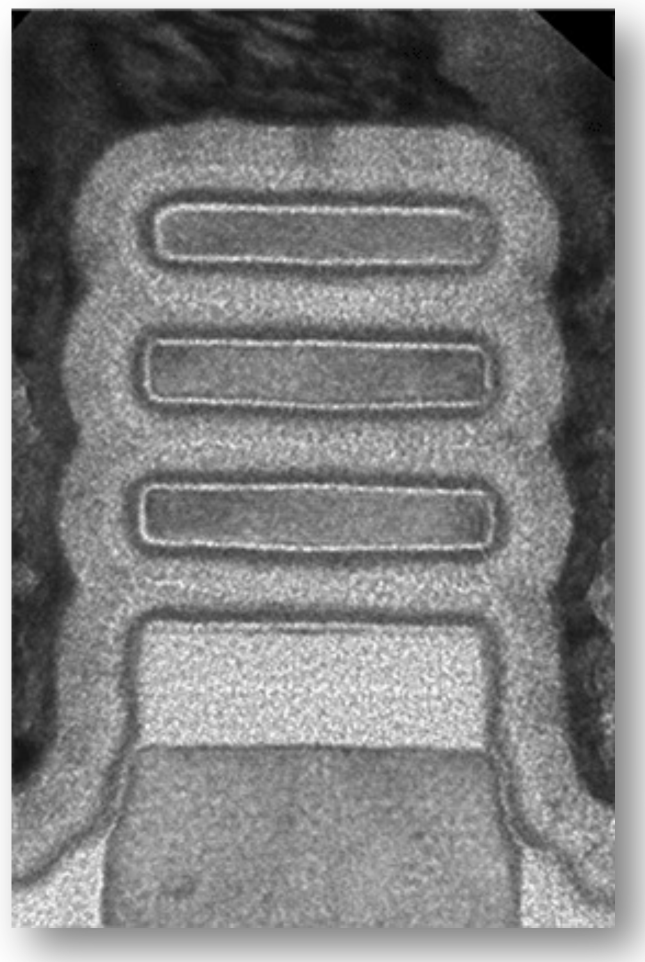
LTLT

Low Temperature Logic Technology

Nanosheet for high performance low temperature electronics for USG systems and requirements

1. Optimized for operation at a temperature of 77K
2. Enables operation at low power supply voltage to reduce power dissipation



The 2 nm transistor in nanosheet structure

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Inventing What’s Next.

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