ACCELERATING
INNOVATION

CMSE 2024

Reducing Board Surface Area and Improving RF Performance by Embedding Ultra-Thin Capacitors

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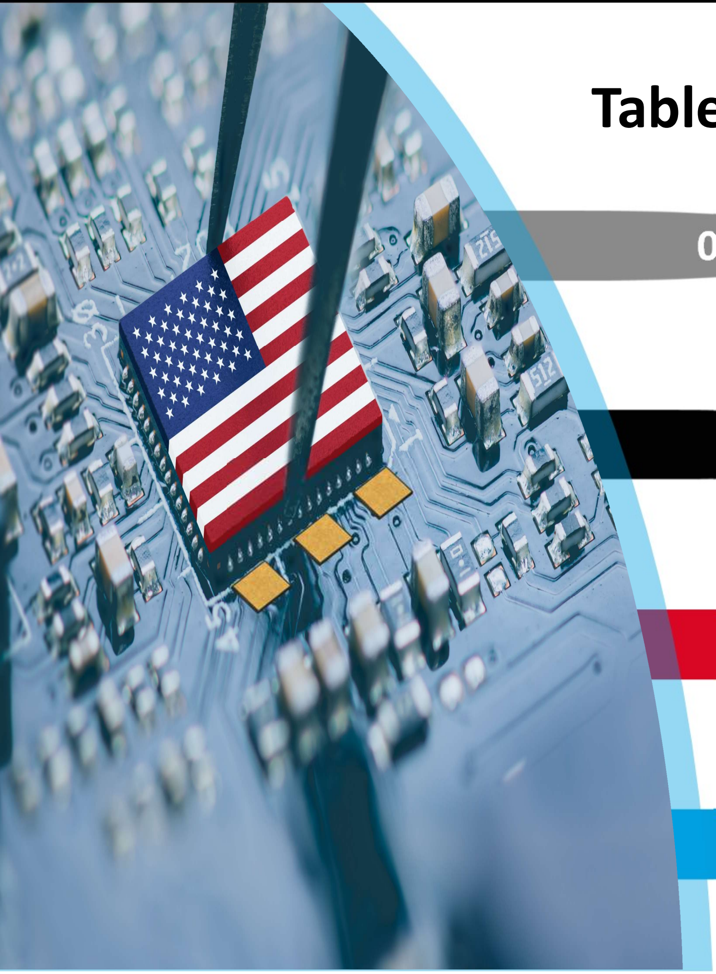
Embedding Ultra-Thin Capacitors



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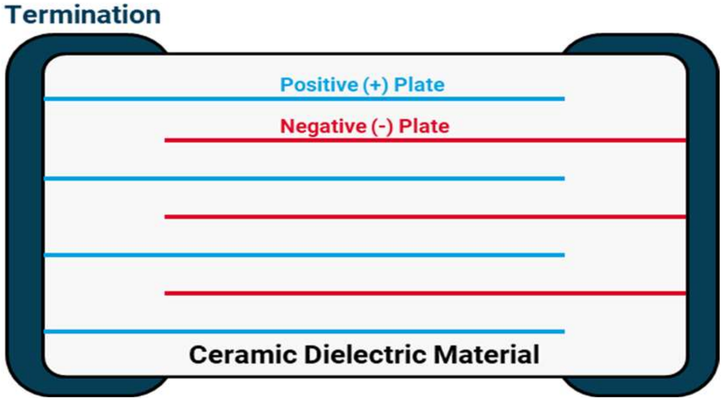
Traditional MLCC Limits

Capacitor Background - MLCC

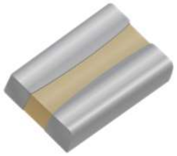
- **MLCC Embeddable limitations**
  - Stacks multiple plates to increase capacitance range, negatively affecting height constraints
  - Surface mount components can be difficult to embed
  - CTE Mismatch issues
  - Chip thickness based on capacitance and number of layers required
    - 01005 size components could be embedded with 5mil thickness
  - Termination limits connections
    - Would prefer to be uniform and copper for embedding
    - Can't be placed on a ground plane without rotating



Cross section of a traditional surface mount capacitor with multiple plates with 1 terminal shown with blue plates and the other with red plates

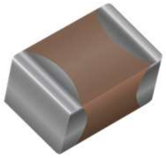
General Embedding Solutions

Current Embedding Solutions in the marketplace

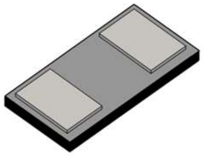


MLCC-2T RGC Capacitor

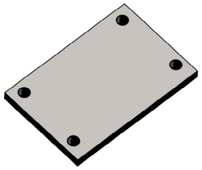
MLCC-3T Capacitor



Std MLCC-01005

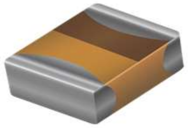


2T Silicon Capacitor



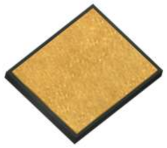
Silicon Array Capacitor

Digital Applications

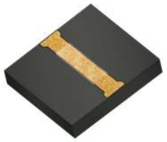


Frameless Tantalum Capacitor

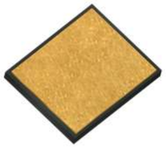
SLC-MIS Capacitor



SLC-MOS Capacitor



SLC-MIM Capacitor

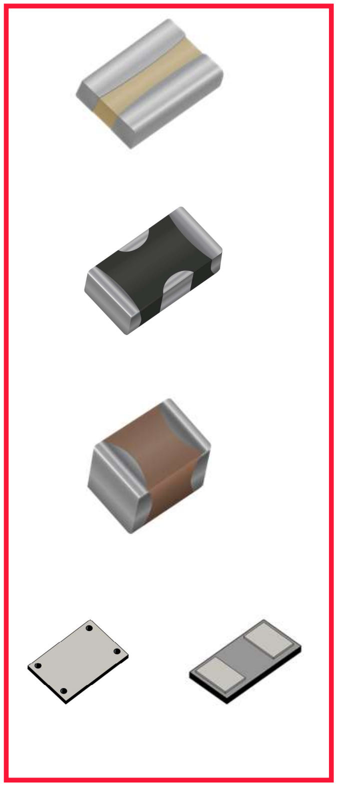


Single Layer Resistor Capacitor

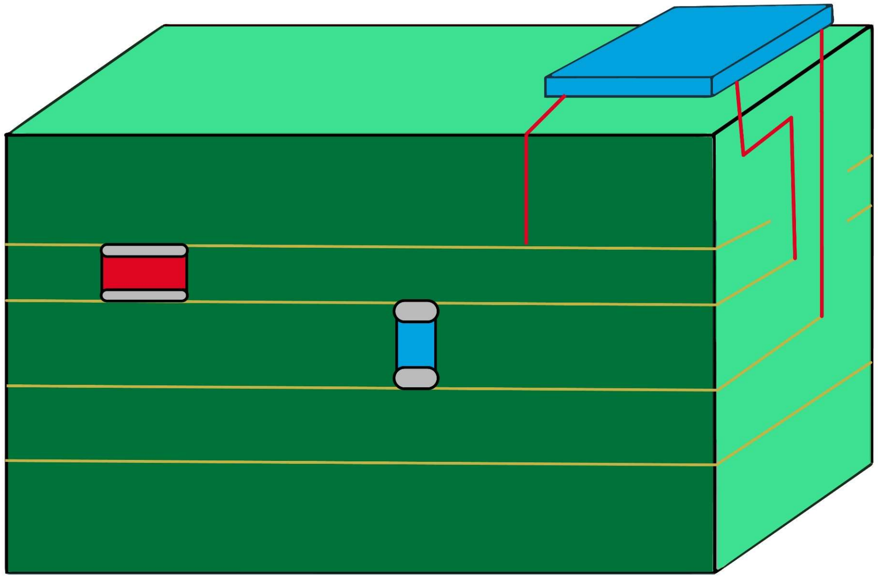
RF Applications

Digital Embedding-MLCC

Current line up

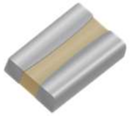
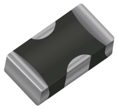
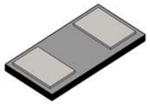
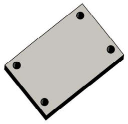
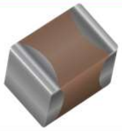


- Ultra Thin, Low Inductance, Large Capacitance, Improved Filtering
- Can further reduce components with the use of Feedthru Caps, Improved Filtering, Hi CV
- Ultra Thin, Low Inductance, Large Capacitance, Improved Filtering
- Thinnest option, CTE match with board, but lower max voltage and not practical in all solutions

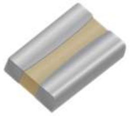
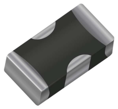
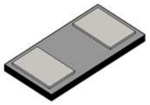
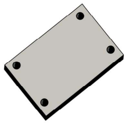


Digital Embedding Specs

Current Embeddable Lineup-Digital

	2T RGC	3T	2T Silicon Cap	Siclicon Cap Array	Std MLCC (01005)
					
L x W	1.0 x 0.5 mm	1.0 x 0.5 mm	1.0 x 0.5 mm	2.53 x 0.6 mm	0.4 x 0.2 mm
Max Thickness	0.3 mm	0.5 mm	0.15 mm	0.165 mm	0.22 mm
Capacitance	0.1 µF	4.3 µF	0.21 µF	0.67 µF	0.47 µF
Dielectric	X7R	X6S	Equivalent to C0G	Equivalent to C0G	X5R
R.V.	4 V	4 V	4 V	4 V	6.3 V

Proposed Embeddable Lineup-Digital (Low Profile)

	2T RGC	3T	2T Silicon Cap	Siclicon Cap Array
				
L x W	1.0 x 0.5 mm	1.0 x 0.5 mm	1.0 x 0.5 mm	2.4 x 2.0 mm
Max Thickness	0.22 mm	0.22 mm	0.15 mm	0.22 mm
Capacitance	1 µF	1 µF	0.525 µF	4.8 µF
Dielectric	X7R	X6T	Equivalent to C0G	Equivalent to C0G
R.V.	4 V	4 V	2 V	2 V

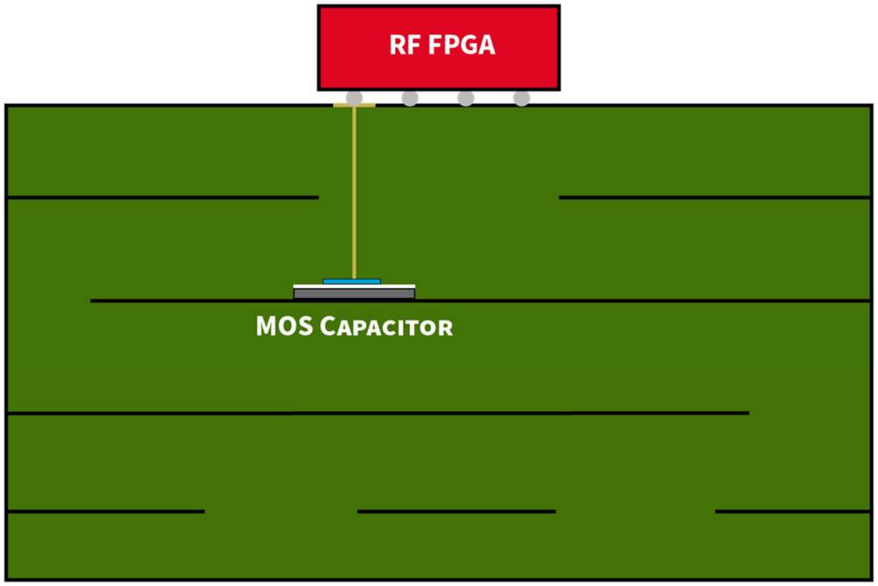
Typical Applications

- **Advanced FPGA GPUs/ASICs**
- **Analog – Digital Converter (ADC)**
- **High-Speed Decoupling**

RF Embedding-SLC

SLC Advantages

- Embedding circuits into the printed circuit board saves space
- Improved frequency response
- RF performance can be improved through proper embedding
- Greatly reduced thickness, wire bondable, ideal ground plane position
- Reduces trace inductance by such a large magnitude that frequency range is extended



RF Embedding-SLC

Capacitor Background – SLC

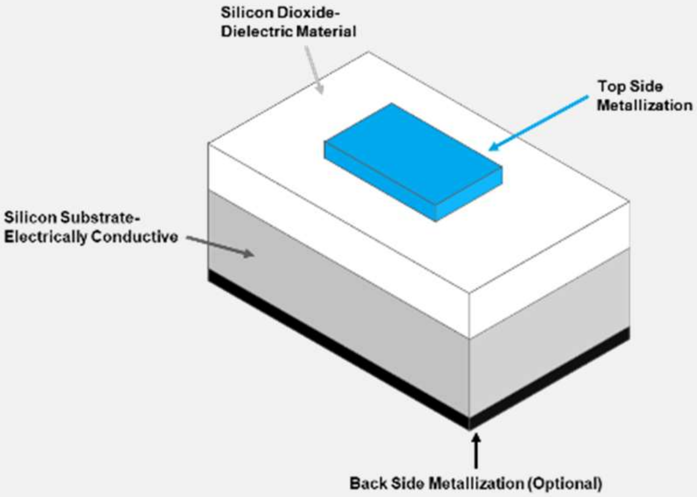
- **Single Layer Capacitor (SLC)**
  - Two plate design
    - Allows backside to be on ground plane
  - Ceramic material changed to change capacitance value
  - Can get high capacitance values in small package
  - Offers ultra-thin thicknesses
- **Embeddable Limitations**
  - Capacitance dependent on thickness/material
  - Materials vary in temperature stability
  - Materials vary in structural match with PCB

Top Cross section of a single layer capacitor the top metallization is represented with a blue line and the backside metallization is represented with a red line. Bottom Render of SLC frontside (with border) and backside

RF Embedding-MOS Cap

Capacitor Background – MOS Capacitor

- **Metal Oxide Silicon (MOS) Capacitor**
  - Two plate design
    - Subset of the SLC capacitors
  - Silicon substrate
    - Improves temperature performance and board match
    - Ultra-thin design below 5 mil
  - Oxide layer for dielectric
    - Can vary thickness without affecting chip thickness
  - Ideal for copper termination plating
- **Embeddable Limitations**
  - Cap values limited vs same size SLC



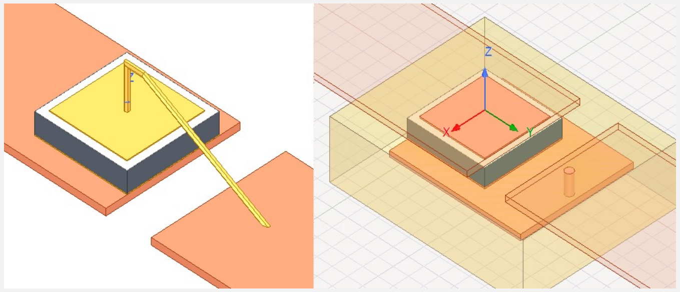
Cross section of metal oxide silicon capacitor with blue line for top side metallization and black line for backside metallization

RF Embedding-MOS Cap

Modeled Performance

– Wirebond vs Embedded

- **Modeled performance in Ansys HFSS**
- **Wirebond Model**
  - MOS Capacitor with wirebond connection bridging gap between transmission lines
- **Embedded model**
  - MOS Capacitor with via from transmission line to capacitor
  - Internal trace beyond the capacitor size connecting backside
  - Via from internal trace to top side transmission line
  - Epoxy used for the material where the embedding happened
- **Transmission lines and board remained same other than noted changes**
  - Rogers 4350, 50 ohm lines

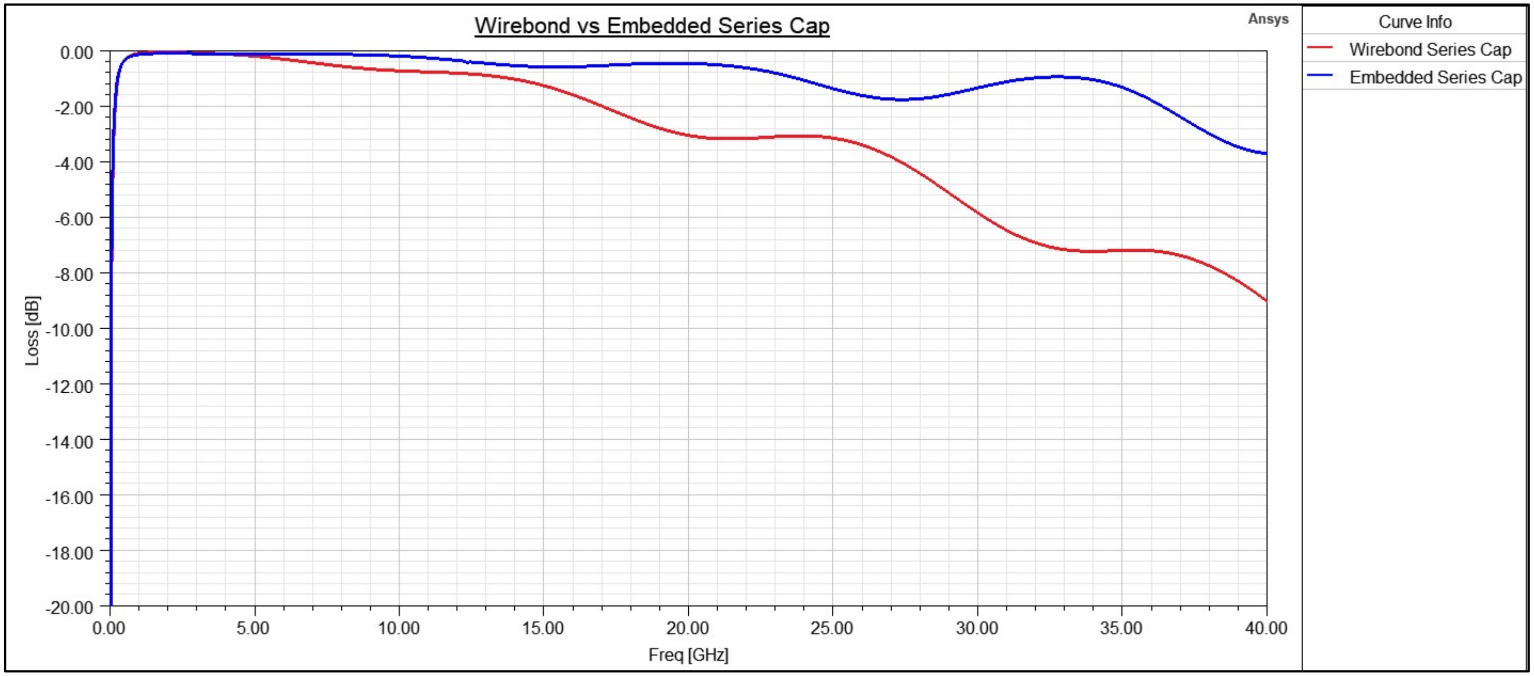


Left: 10pF MOS capacitor on Rogers 4350 test board with wirebond connection. **Right:** 10pF MOS capacitor embedded in epoxy filled Rogers 4350 test board with via to transmission line.

RF Embedding-MOS Cap

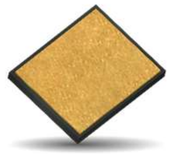
Model - Wirebond vs Embedded - Results

- Wirebond degrades at 5 GHz
- Cap performance extends beyond 20 GHz with minimal loss with embedded method



Typical RF SLC Offering

	MV Series	
	MIM	
Temperature	-55°C to +125°C	
Frequency	≤ 100 GHz	
Rated Voltage	100 V_{DC}	
Thickness	5 MIL	10 MIL
30 x 40		15 pF
40 x 20	15 pF	
40 x 40		15 pF
50 x 50	15 pF	
80 x 20	15 pF	
80 x 40		1 pF & 15 pF
120 x 40		15 pF



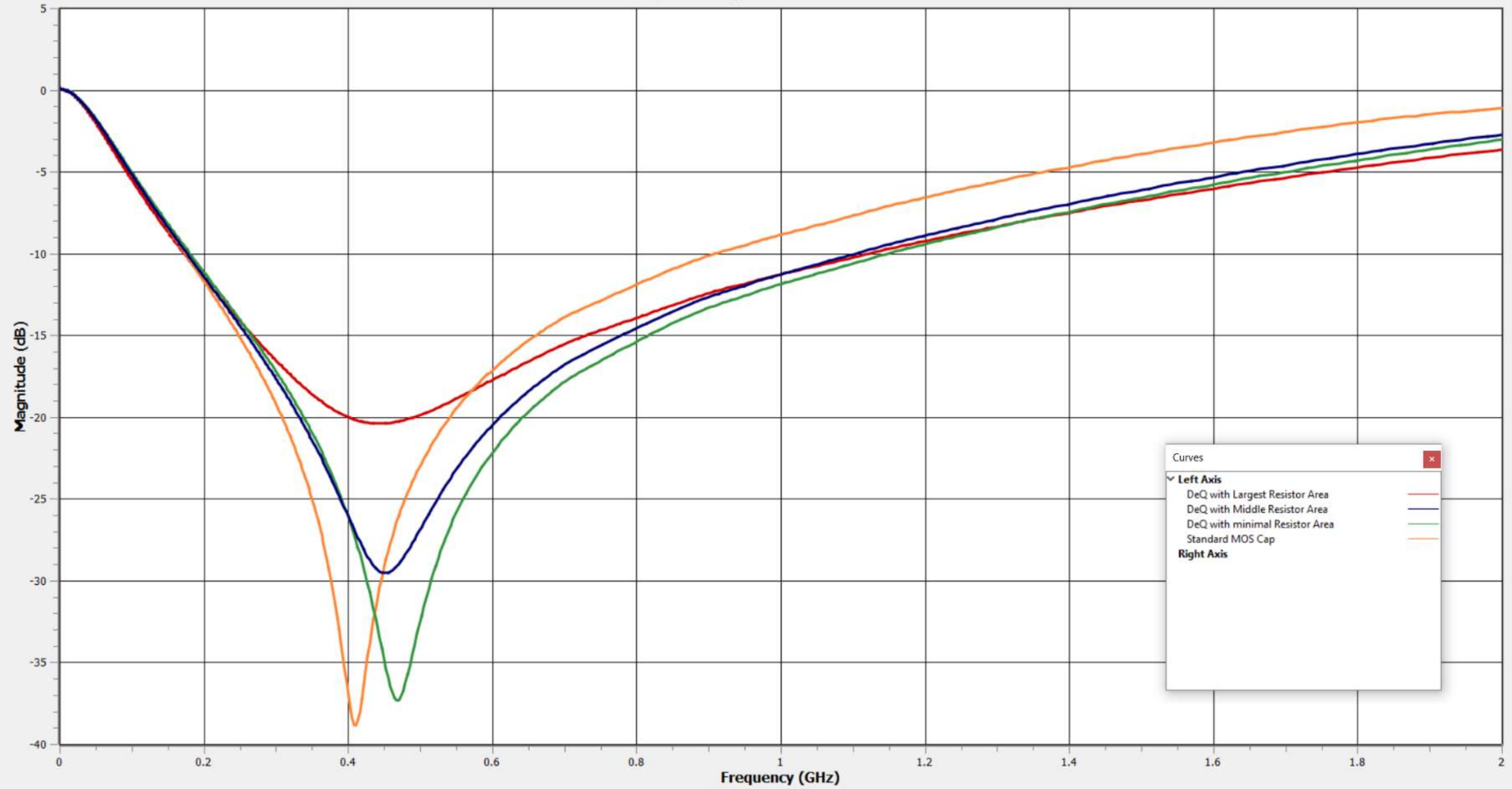
	MS Series	
	MOS	MIS
Temperature	-55°C to +125°C	
Frequency	≤ 100 GHz	
Rated Voltage	25 - 200 V_{DC}	
Thickness	5 - 10 MIL	
10 x 10	1 - 12 pF	1 - 19 pF
20 x 20	1 - 75 pF	1 - 115 pF
30 x 30	1 - 190 pF	1 - 290 pF
40 x 40	1 - 370 pF	1 - 550 pF
50 x 50	1 - 600 pF	1 - 900 pF
60 x 60	1 - 880 pF	1 - 1320 pF
70 x 70	1 - 1200 pF	1 - 1800 pF

	Ultra Maxi	Maxi		Maxi +		Z Series		Temp Compensating		111 Series
	No Boarders	No Boarders	Boarders	No Boarders	Boarders	No Boarders	Boarders	No Boarders	Boarders	Boarders
Temperature	-55°C to +125°C									
Frequency	≤ 100 GHz									
Rated Voltage	25 V_{DC}	50 V_{DC}				50 & 100 V_{DC}				≤ 100 V_{DC}
Thickness	5.5 - 7.5 MIL	5 - 9 MIL						4.5 - 12 MIL		
10 x 10	200 - 300 pF									
15 x 15	300 - 600 pF	68 - 330 pF	51 - 220 pF	330 - 390 pF	220 - 330 pF	20 - 200 pF	20 - 150 pF	0.06 - 60 pF	0.06 - 33 pF	
18 x 18								0.08 - 75 pF		0.1 - 220 pF
20 x 20	0.55 - 1 nF								0.1 - 62 pF	
25 x 25	0.9 - 1.5 nF	330 - 750 pF	220 - 550 pF	0.39 - 1 nF	330 - 820 pF	35 - 470 pF	30 - 390 pF	0.2 - 150 pF	0.2 - 100 pF	0.2 - 510 pF
30 x 30	1.4 - 2 nF								0.3 - 150 pF	
35 x 35	1.9 - 2.7 nF	0.75 - 1.2 nF	0.56 - 1 nF	1 - 1.8 nF	0.82 - 1.5 nF	80 - 800 pF	70 - 700 pF	0.4 - 300 pF	0.4 - 200 pF	0.4 - 910 pF
40 x 40	2.6 - 3.5 nF								0.5 - 270 pF	
45 x 45	3.3 - 4.4 nF									
50 x 50	4.2 - 5.4 nF	1.2 - 2.7 nF	1 - 2.2 nF	1.8 - 3.3 nF	1.5 - 2.7 nF	0.15 - 2 nF	0.14 - 1.8 nF	0.6 - 680 pF	0.8 - 430 pF	0.6 - 2200 pF
55 x 55	5.1 - 6.5 nF									
70 x 70		2.7 - 4.7 nF	2.2 - 4.7 nF	3.3 - 6.8 nF	2.7 - 6.8 nF	0.3 - 3 nF	0.28 - 2.7 nF	1.3 - 1200 pF		1.3 - 3900 pF
90 x 90		4.7 - 8.2 nF	4.7 - 8.2 nF	6.8 - 10 nF	6.8 - 10 nF	0.5 - 4.7 nF	0.47 - 4.5 nF	2.2 - 1800 pF		2.4 - 6200 pF

NPI: Single Layer Resistor Capacitor (SLRC)

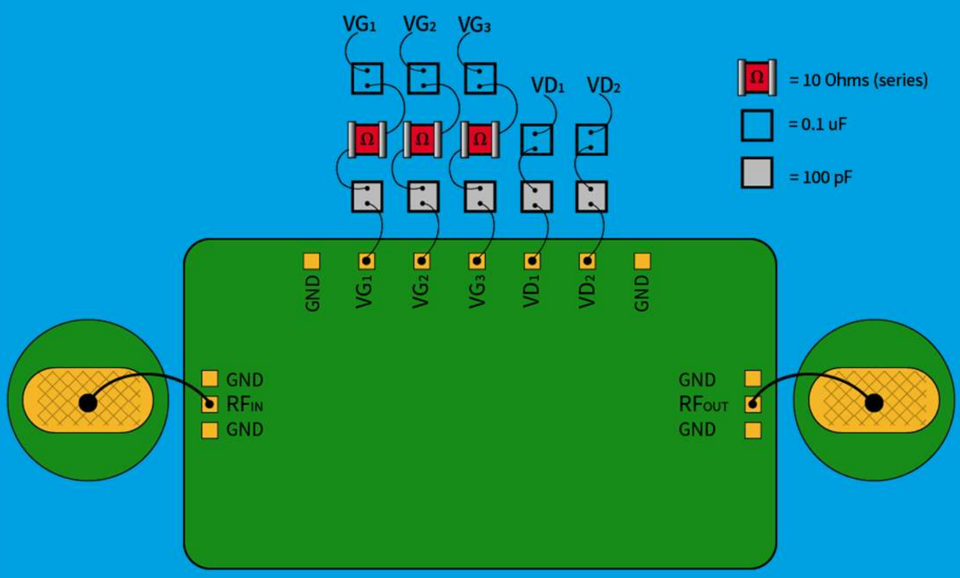
	MR Series	
	MR	
		
Temperature	-55°C to +125°C	
Frequency	≤ 100 GHz	
Rated Voltage	25 - 200 V_{DC}	
Thickness	5-10 MIL	
10 x 10	1 - 12 pF	1 - 19 pF
20 x 20	1 - 75 pF	1 - 115 pF
30 x 30	1 - 190 pF	1 - 290 pF
40 x 40	1 - 370 pF	1 - 550 pF
50 x 50	1 - 600 pF	1 - 900 pF
60 x 60	1 - 880 pF	1 - 1320 pF
70 x 70	1 - 1200 pF	1 - 1800 pF

DeQ Single Layer Resistor Capacitor

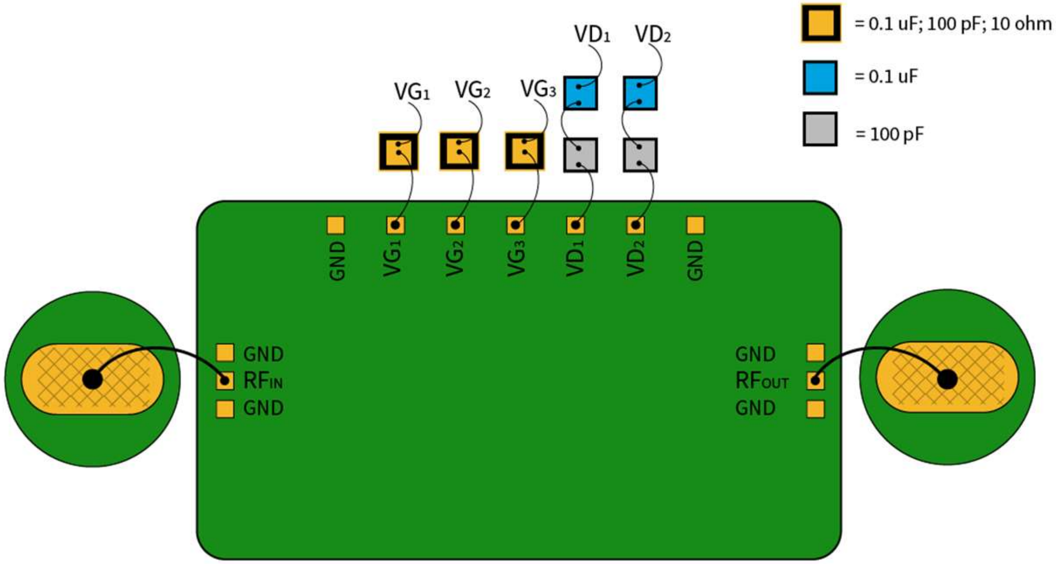


RF Application: SLRC

Traditional configuration for LNA MMIC



Optimized configuration for LNA MMIC utilizing SLRC



Embedding Passive Components

Summary

- **The Industry is moving towards embedding passive components to reduce board space**
- **Embedding SLC or MOS Capacitors reduces board footprint**
  - SLC and MOS are very customizable devices to fit the needs of your system
  - Arrays give flexibility and can be multiple capacitance values
  - Using vias, they can be mounted in a variety of ways
- **Removing the wire bond creates an RF performance boost**
  - Even compared to surface mount components
- **Wide Array of Component Suppliers are offering embeddable solutions**
- **New Parts are being introduced to facilitate the need to reduce board space (SLRC)**
  - Most passive component suppliers will be introducing these parts in the near future

THANK YOU.

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