Heterogeneous Integration Roadmap

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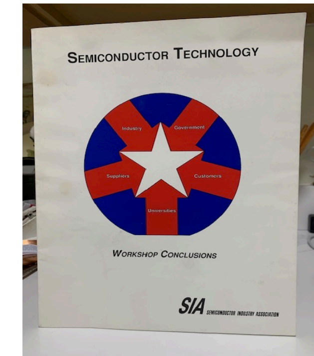
The Technology Roadmap
Creating a Common Vision and Collaboration

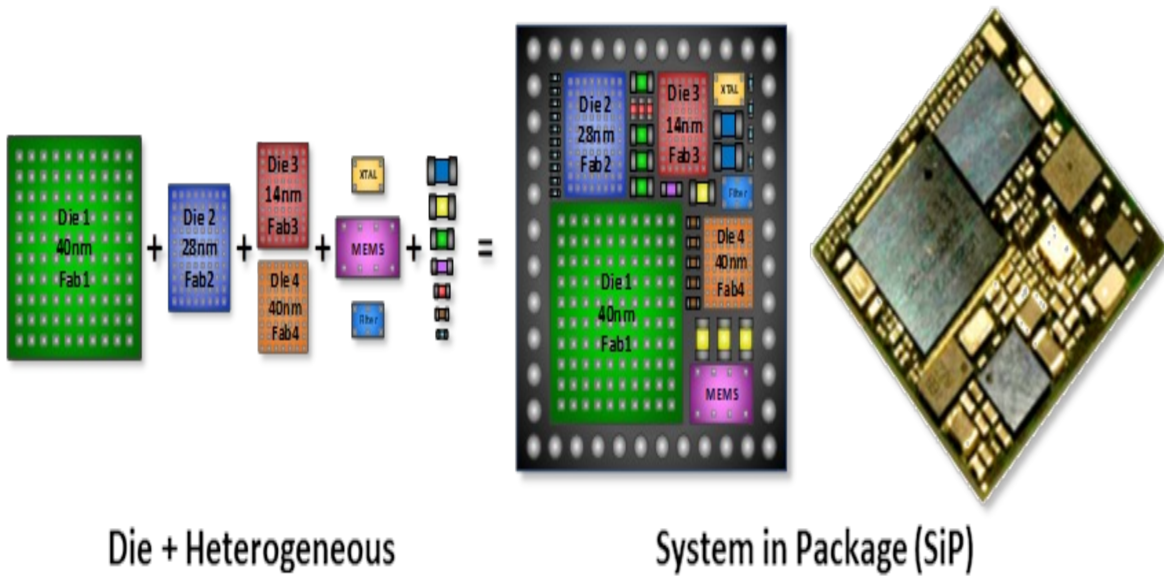
The National Technology Roadmap for Semiconductors (NTRS) was initiated by SIA Technology Committee chaired by **Dr Gordon Moore**. He invited 179 technologists to a workshop in Irving Texas to create a common vision and collaboration of semiconductor technology over the next 15 years across industry, suppliers, customers, academia, government & national laboratories.. The report published in 1993 constitute the first open-source Semiconductor Technology Roadmap.

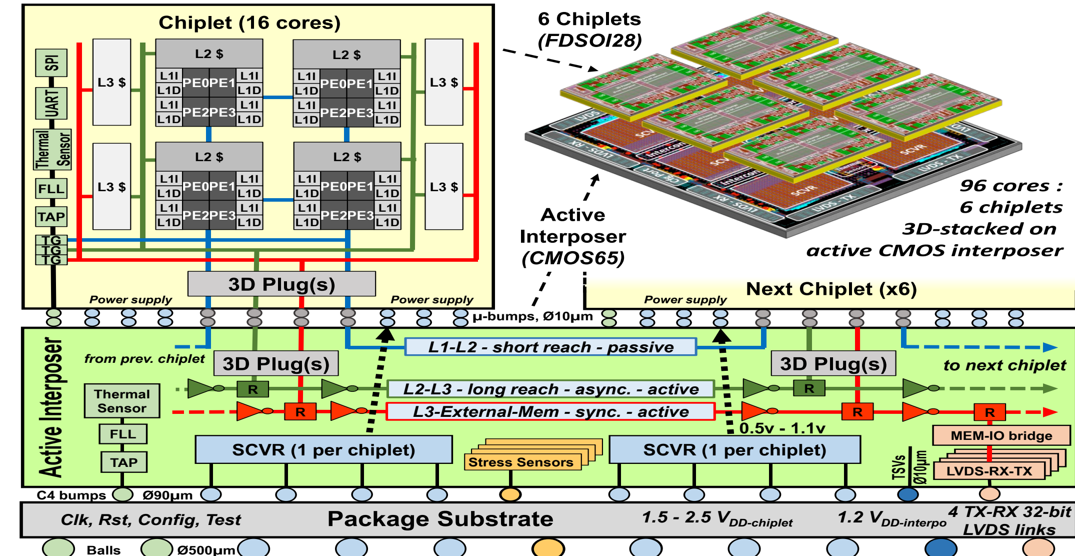


In 1998 the NTRS roadmap work was joined by four other regional Semiconductor Industry Associations: Taiwan, South Korea, Japan and Europe to become International Technology Roadmap for Semiconductors (ITRS), In 2014 decision was made by SIA to end ITRS. The last edition of ITRS was published July 8, 2016.

The Heterogeneous Integration team in ITRS in 2014 learnt of the closure of ITRS decided to continue the Technology Roadmap effort towards shared vision and collaboration for the next era of Moore's Law progress for Electronics Resurgence into the Future Decades.

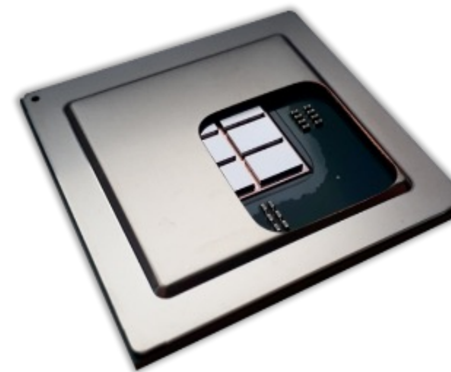
The Definition of Heterogeneous Integration

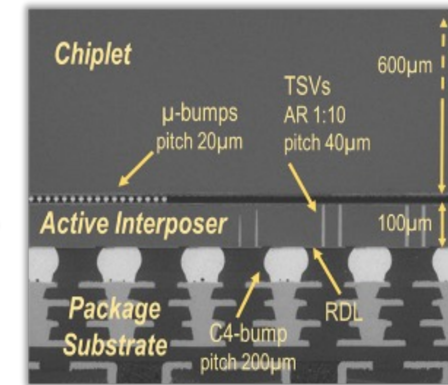




Heterogeneous by multi-scale and multiphysics:

- Material
- Component type (IC, Photonics, MEMS, sensors)
- Circuit type (DRAM, Serdes, logic, RF, Power)
- Si Node
- Level/method of bonding/interconnection



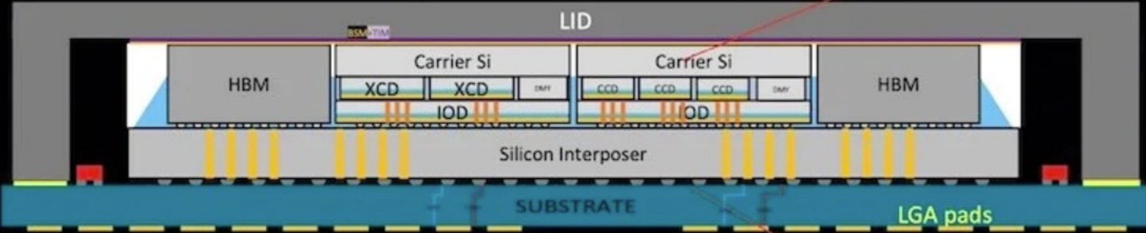


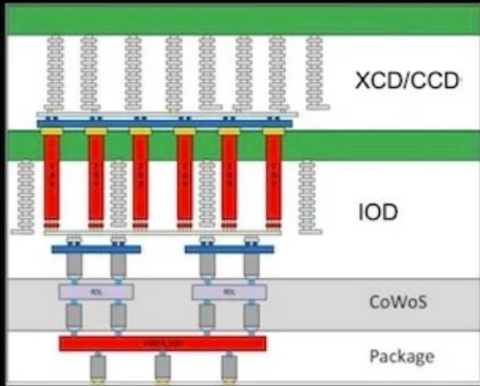
Source: 2020 ISSC

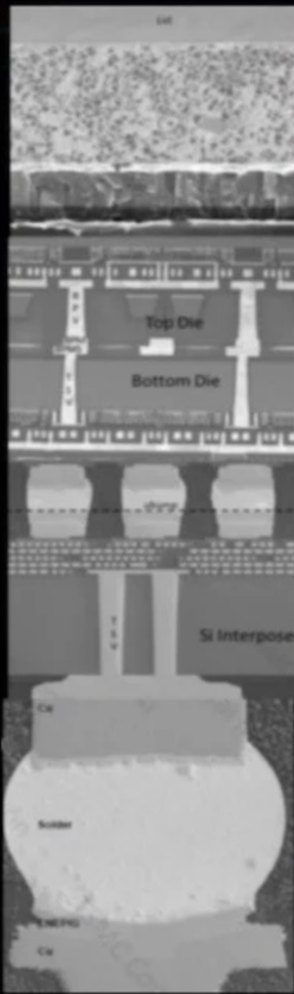
AMD 3.5D Advanced Packaging

AMD Instinct™ MI300 Family

3.5D Advanced Packaging







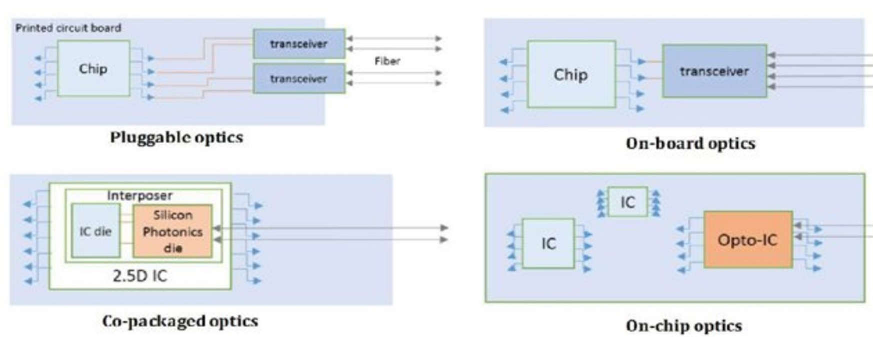
3D Hybrid Bonded Architecture compute density and perf/W

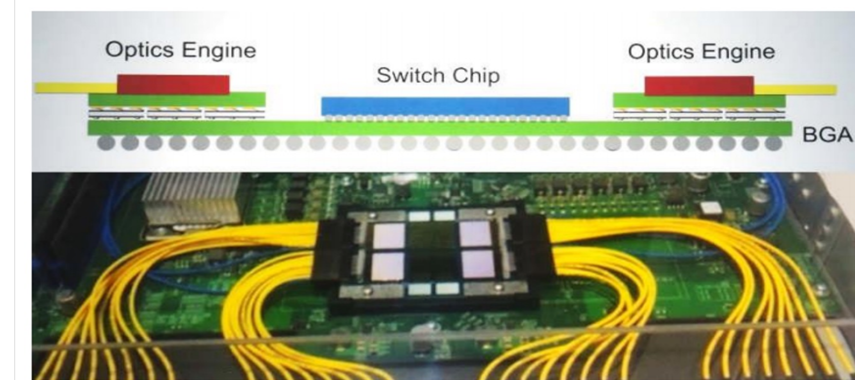
2.5D Architecture for IOD-IOD and HBM3 integration

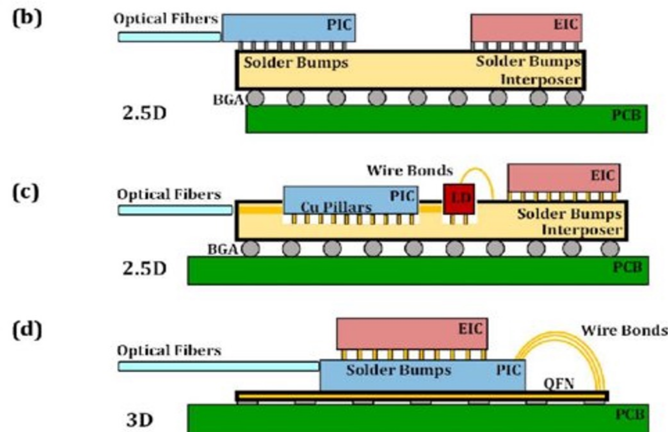
Large module on substrate

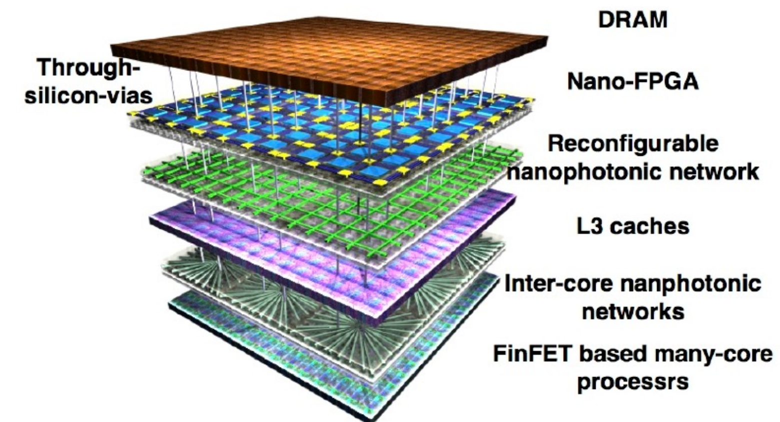
Heterogenous Integration of Electronics and Photonics

- Evolution of Photonics Packaging
  - Heterogenous integration of passive/active photonics devices and IC devices from board level to package and wafer levels
  - Co-Packaged Optics (CPO) Using 2.5D and 3D Packaging technology









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Heterogeneous Integration Roadmap (HIR)

23 Chapters Covering total Microelectronics Systems & Technology Ecosystem

HIR
HETEROGENEOUS INTEGRATION ROADMAP

HI Systems & Market Applications

- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Cross Cutting topics

- Materials & Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management
- **Reliability**

Heterogeneous Integration Components

- Single Chip and Multi Chip Integration (including Substrates)
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor integration
- 5G Communication & Beyond

Integration Processes

- SiP & Module
- 3D +2D & Interconnect
- Wafer Level Packaging (fan in and fan out)

Co-Design + Simulation

- Co-Design
- Modeling & Simulation

White Papers Stage: Additive Manufacturing and Quantum

Hardware Reliability Topic Matrix

- Reliability road-map of HI systems requires coordination across all TWGs

<table>
<tr><th></th><th>Reliability Targets</th><th>Life Cycle Conditions</th><th>Design for Reliability</th><th>Manufacturing for Reliability</th><th>KBT[4] for Reliability Qualification: EV/DV/PV[1]</th><th>PHM[5]</th><th>Supply Chain</th></tr>
<tr><td>SiP Technologies</td><td colspan="2">TWGs: SCM/MCM , Photonics, MEMS, Power, RF/Analog</td><td rowspan="3">TWGs: Electromigration; Materials; Co-Design and Simulation Topic Teams: Electrical System Performance; Thermal Management; Mechanical Structure and Mechanics</td><td>TWGs: SCM/MCM; Photonics; MEMS/Sensors; Power; RF/Analog; Test</td><td rowspan="3">Test TWG</td><td rowspan="3">Security TWG</td><td rowspan="3">Supply Chain TWG</td></tr>
<tr><td>Package Integration</td><td colspan="2">TWGs: WLP, 2.5D/3D, Interconnects, SIP Topic Teams: WST; Substrate</td><td>TWGs: WLP; 2.5D/3D; Interconnects; SIP, Test; Topic Teams: WST; Substrate; Board Assembly</td></tr>
<tr><td>Applications</td><td colspan="2">TWGs: Mobile, IoT, MHW, Automotive, HPC, Aerospace</td><td>TWGs: Mobile; IoT; MHW; Automotive; HPC; Aerospace; Test</td></tr>
</table>

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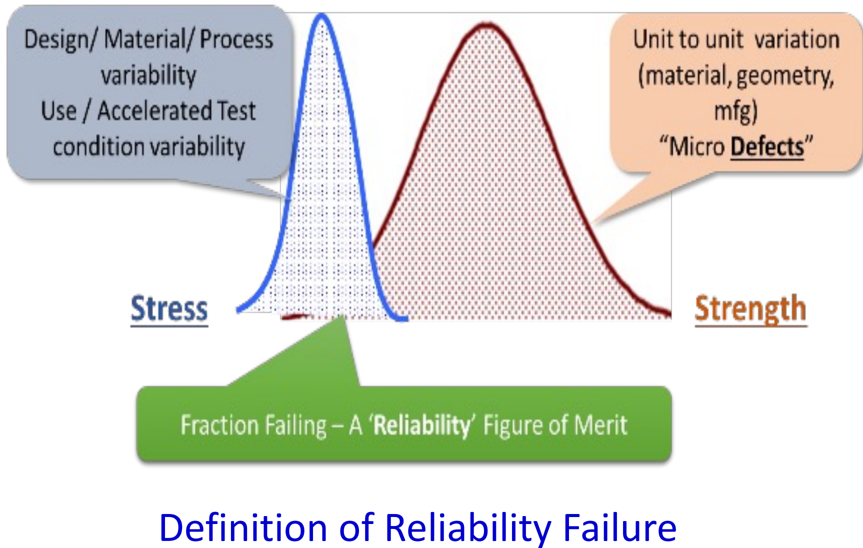
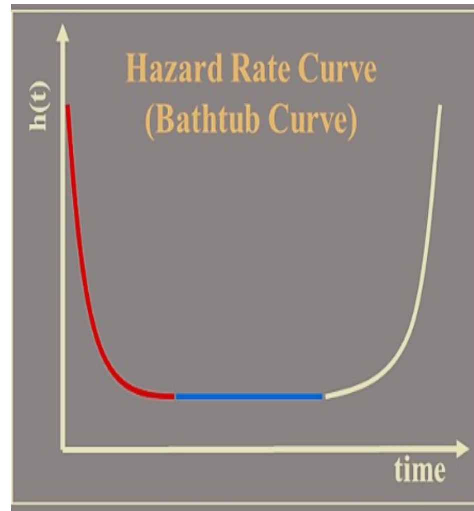
Heterogenous Integration System Reliability Introduction

- Systems with heterogeneous integration (HI) will experience new multiscale chip-package interactions and multi-physics failure modes
- Managing reliability of HI systems will require holistic cradle-to-grave methodology

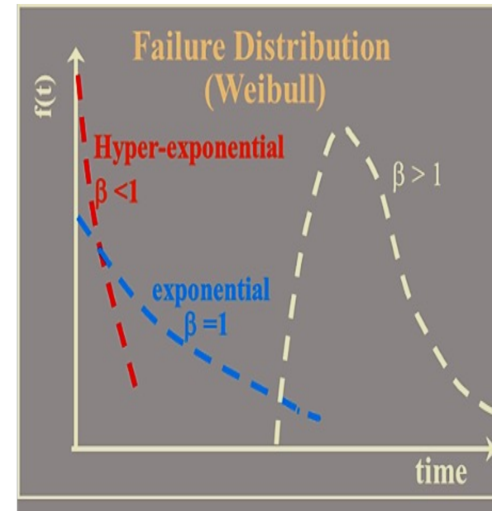
- HI system reliability depends on aggregation of multiple degradation modes



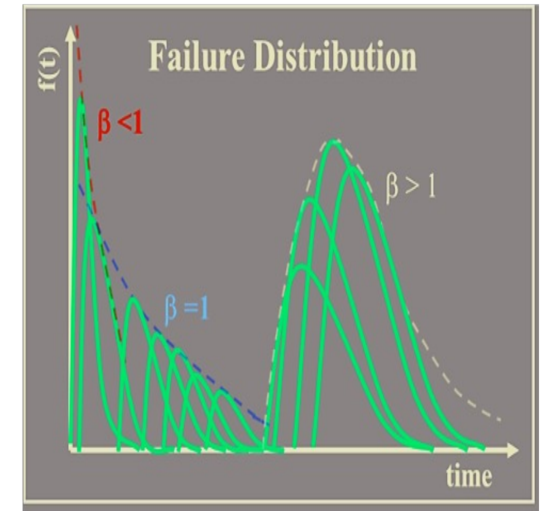
Definition of Reliability Failure



Typical Bathtub Curve based on hazard rates



System-level Bathtub Curve expressed as Weibull Failure Distribution



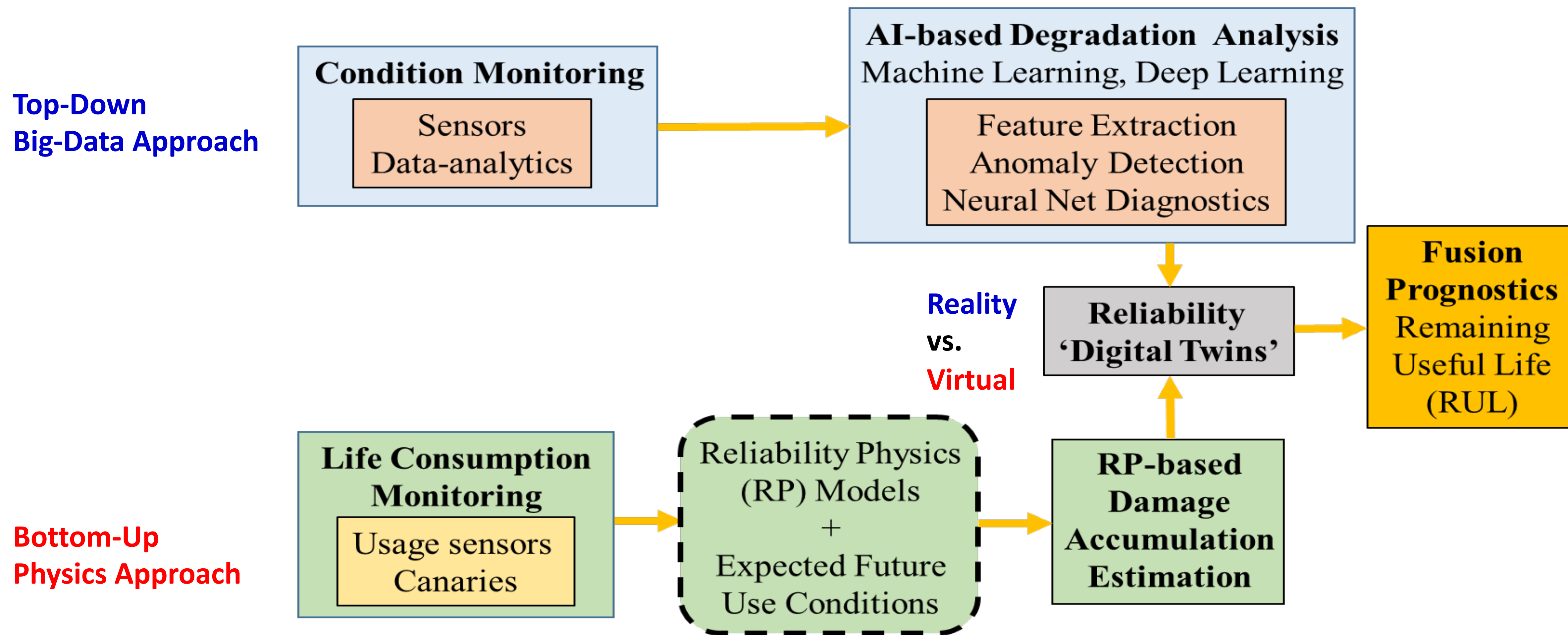
HI Systems Bathtub curve is the result of Multiple Competing Failure Modes

- In this era of Chiplets and multi-devices packages, innovations and collaborations in Reliability Technology and Science will be crucial for the semiconductor and microelectronics industries decades into the future.

Reliability Methodology of HI Systems

HIR
HETEROGENEOUS INTEGRATION ROADMAP

- ‘Digital Twins’ for managing reliability will rely on fusion methods that combine bottom-up physics and top-down big-data approaches



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Reliability Challenges: Future Outlook

		Reliability Targets	Life Cycle Conditions	Design for Reliability	Manufacturing for Reliability	Qualification for Reliability	Sustainment for Reliability	Supply Chain
Applications	Mobile							
	IoT							
	Medical, Health and wearables							
	Automotive							
	HPC & Data Centers							
	Aerospace and Defense							
Package Integration	WLP (FO/FI)							
	2.5D and 3D integration							
	Wafer Singulation and Thinning							
	Chip-package interactions (CPI)							
	Interconnects (TSV8s, μbumps, wirebonds, Flip Chip solder joints)							
	Substrates/Interposers							
	Board Assembly							
	SOC/SIP/SOP[9] formats							
Technologies	Microelectronics > 10 nm							
	Microelectronics <10 nm							
	Photonics & optics							
	MEMS and sensors							
	Power electronics							
	Energy souces (Batteries/PV[6]/FC[7])							
	RF/Analog Devices							

1-5 Years:

Multi-physics fusion approaches for reliability assurance

- Bottom-up *Reliability Physics* based approaches, tools, infrastructure
- Top-down *Machine Learning & AI* based approaches, tools, infrastructure

5-10 Years:

Fusion approaches for co-design (based on ‘digital twins’) and life-cycle PHM of next-gen robust HI systems

- Fault-tolerant systems
- Resilient systems

10-15 Years:

Fusion approaches for intelligent, adaptive, reconfigurable products with integrated autonomous life-cycle management capability

- Intelligent, self-cognizant systems
- Self-healing systems

Advanced Thermal Technologies & Research

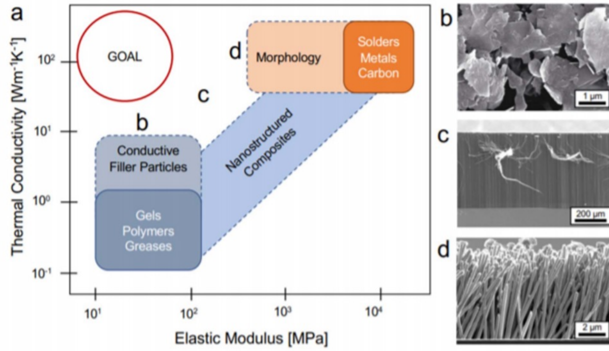
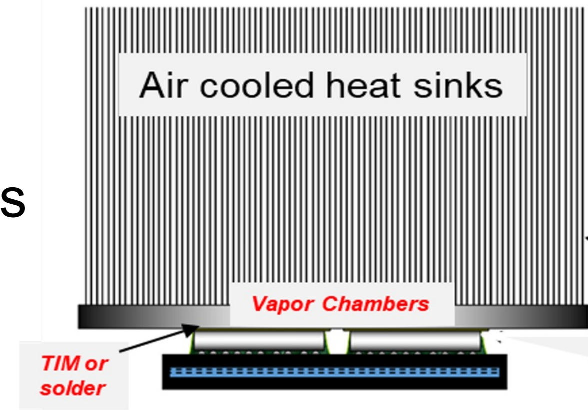
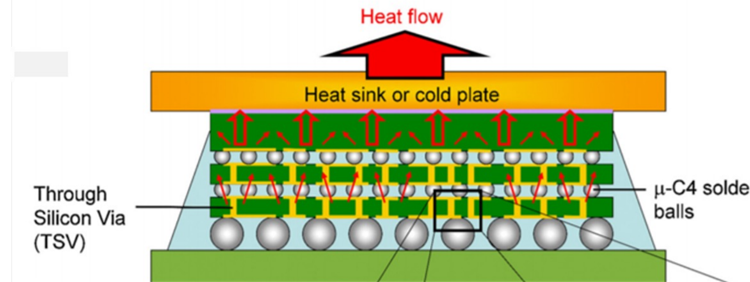


Figure 17 (a) Two common strategies can be employed to create high-performance TIM composites [14], (b) an example of graphene-polymer composite [15], (c) vertically grown nanotubes [16-17], (d) vertically electrodeposited nanowires [14, 18]

[A] Thermal Interface Materials

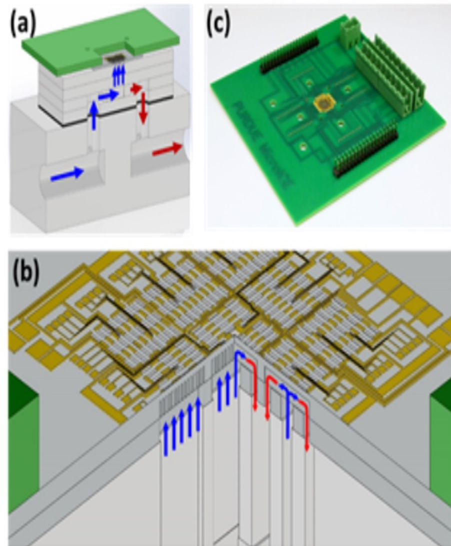
[B] System thermal limits for HPC multi-chip modules





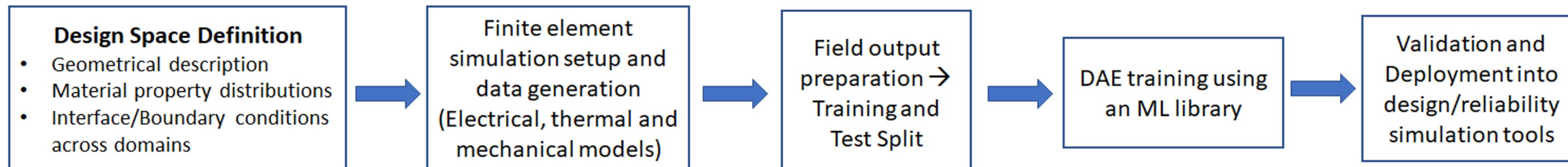
A 3D chip stack using advanced materials in the conduction heat flow path.

[D] Advanced Thermal Materials for Thermal Management



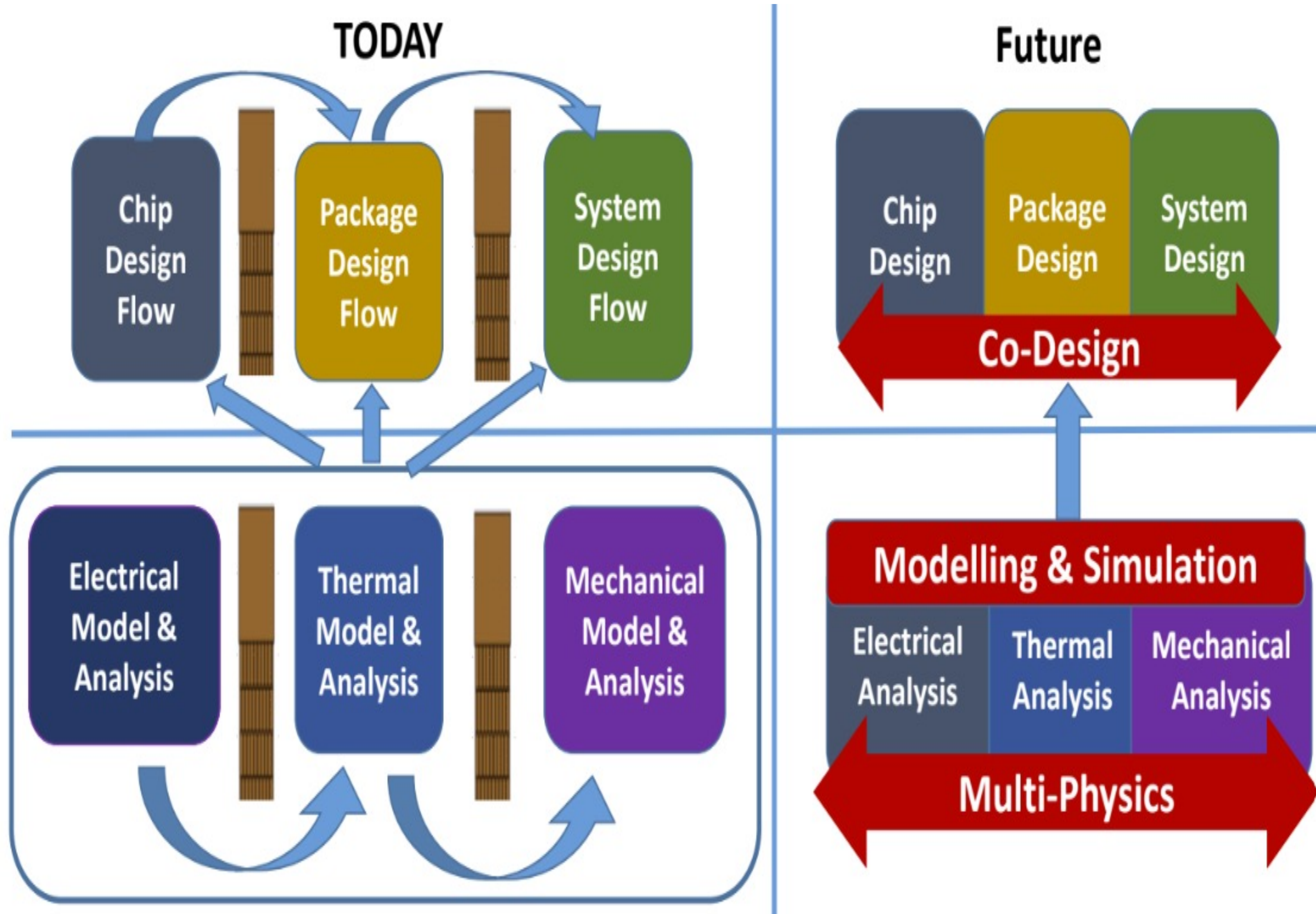
[C] Embedded liquid cooling of chip and chip stacks

[E] Thermomechanical Modeling for Heterogeneous Integration



Modelling and Simulation Techniques

- Electrical analysis
- Thermal & thermomechanical
- Mechanics & multiphysics modeling
- Multi-scale modeling
- Machine learning/AI
- System-level modeling
- Material characterization



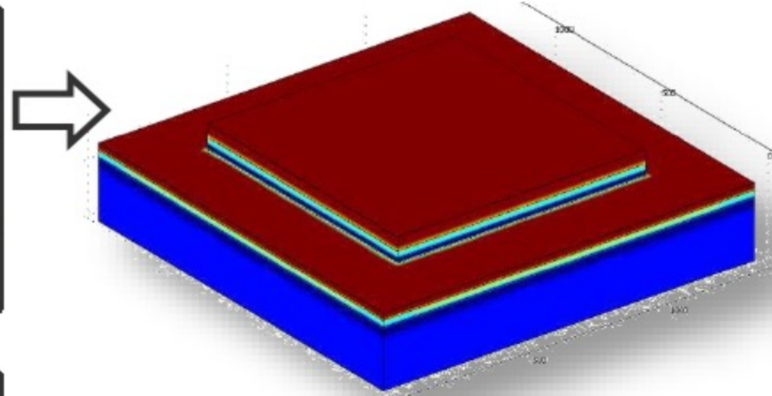
Co-Design Contents

- Components of Co-Design
  - Placement & routing, architecture
  - Electromagnetics and electrical
  - Thermal management
  - Intelligent materials
  - Test
  - Reliability, testing, mechanical
- Infrastructure and Research Needs
  - University research (funding, workforce,…)
  - Shared resources (open source, standards,…)

Multi-Scale and Multi-Physics CPI Flow

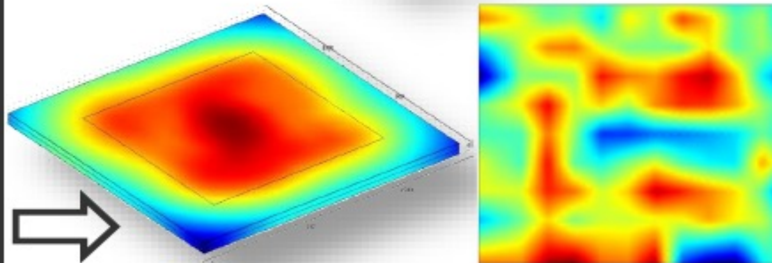
Package-scale simulation (FEA)
Input: geometry; material properties; smeared mechanical properties for RDLs, Silicon/TSV bulk, interconnect.

Output: field of displacement components on the die faces.



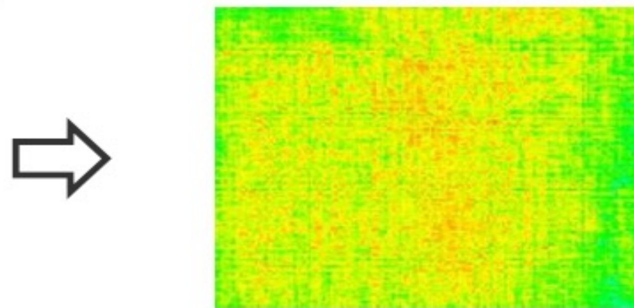
Die-scale simulation (FEA)
Input: geometry; field of displacements on the die faces; coordinate-dependent mechanical properties for RDLs, Silicon/TSV bulk, interconnect.

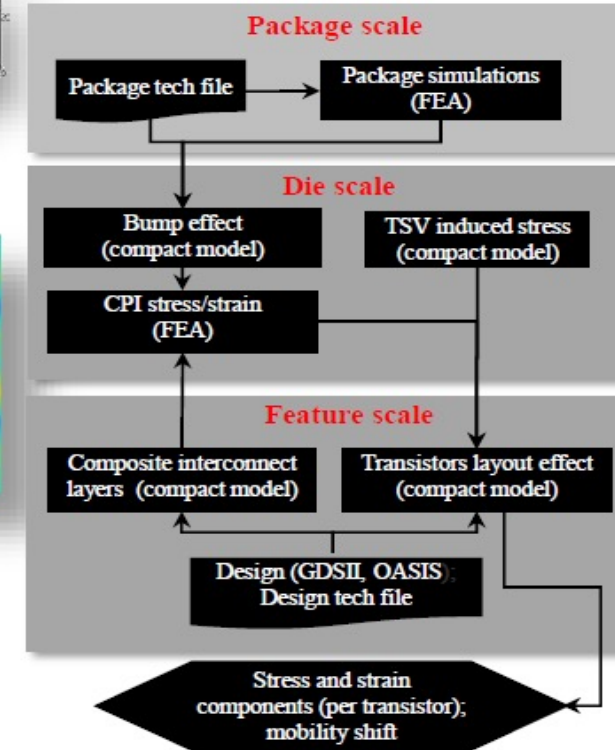
Output: Distribution of the strain components across device layer.



Layout-scale w/feature-scale resolution (compact model):
Input: GDS; distribution of the strain components across device layer.

Output: Transistor-to-transistor variation in stress components





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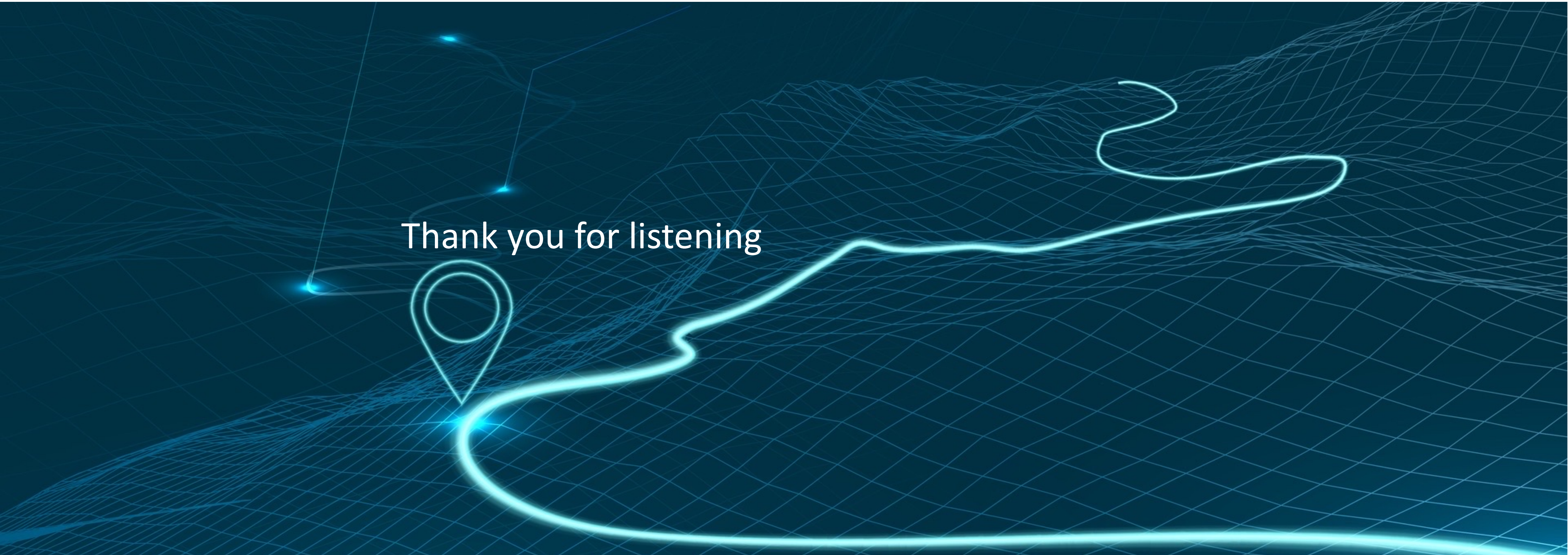
“For while we have our eyes on the future, history has its eyes on us”

Amanda Gorman, Poet Laureate



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