

TIME DEPENDENT CAPACITANCE DRIFT OF X7R MLCCS UNDER EXPOSURE TO A CONSTANT DC-BIAS VOLTAGE



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Time Dependent Capacitance Drift of X7R MLCCs Under Exposure to a Constant DC-Bias Voltage

- Abstract: Until recently, it was assumed that multilayer ceramic capacitor (MLCC) manufacturers' data stating the typical voltage coefficient of capacitance (VCC) and capacitance loss due to aging (no bias) could be additive, and that further capacitance drift over time will not be significant. However, recent research of the capacitance changes of X7R MLCCs under exposure to a constant DC bias voltage has shown that a time-related capacitance drift exists that can be much larger than the typical VCC and normal aging effect combined. This was first questioned by an automotive manufacturer and reported as an issue in critical systems that was related to capacitance loss and bias aging. A study of the DC Bias aging for a very common MLCC (0603 X7R 100nF 50V) was performed which subjected the capacitors to DC bias at 40% and 100% of the rated voltage for more than 1000 hours. The capacitance was measured intermittently to measure the drift. Results indicated the construction and/or material system of the part affected the degree of capacitance drift. Recovery of the capacitance after the bias was removed, also tended to depend on this construction.

Background

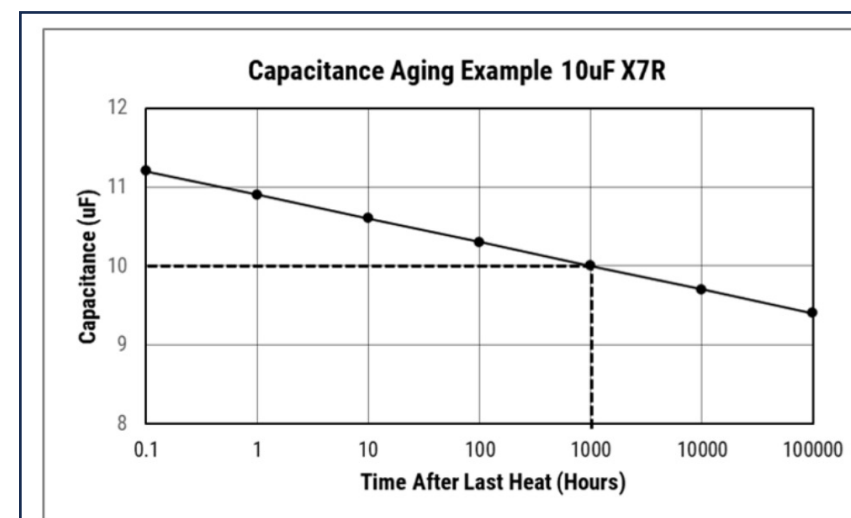
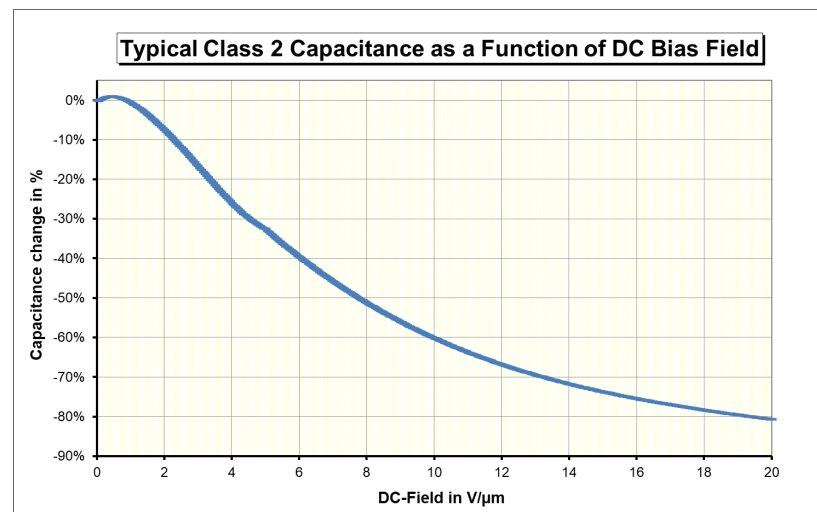
- Multilayer Ceramic Capacitors (MLCCs) offer advantages to the designer:
 - High capacitance, low ESR, low cost, and insensitivity to high temperature assembly
- MLCCs do exhibit changes of their electrical characteristics due to applied voltage and operating temperature, which depends on the nature of the dielectric material used

Class 1 (NP0/COG)	Class 2 (X7R)
<ul style="list-style-type: none"> • Based on paraelectric ceramic + Stable, low loss dielectric material + Very limited effect of voltage and temperature. - Downside: lower dielectric constant → lower available capacitance for a given size 	<ul style="list-style-type: none"> • Based on ferro-electric ceramic compositions. + Higher dielectric constant → higher capacitance values - Downside: capacitance is affected by operating environment

- Because of the high stability of the electrical characteristics and relatively low capacitance values, capacitors of Class 1 are not subject of this study
- However, several factors affect the stability of the electrical characteristics of Class 2:
 - Temperature, DC-bias voltage, frequency, AC-voltage amplitude as well as aging of capacitance and dissipation factor over time

Background

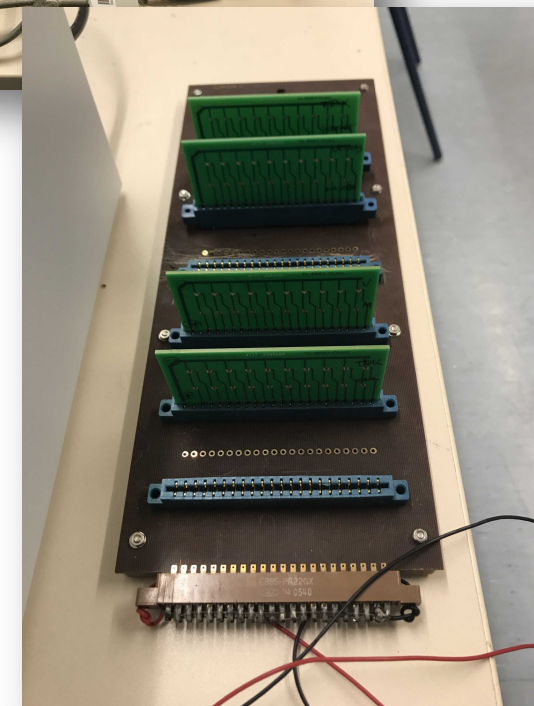
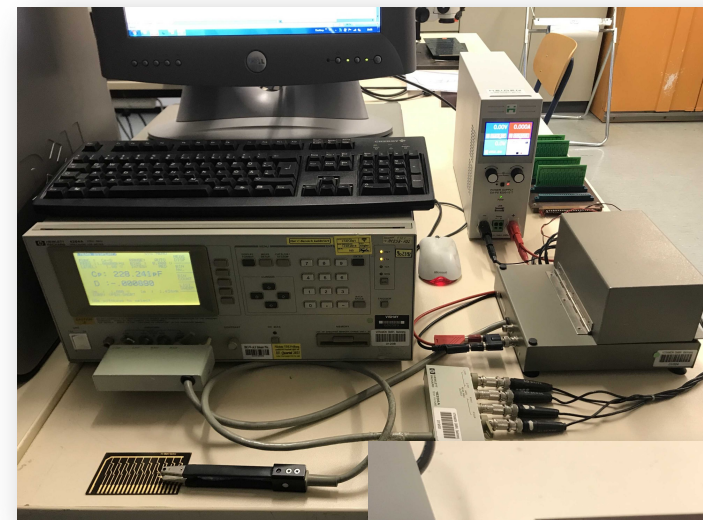
- Until recently, it was assumed that the loss of capacitance in Class 2 MLCCs was due to 3 factors:
 - Application of a DC-bias voltage
 - Aging of the capacitor
 - Temperature
- However, recent reports of the capacitance change over time under the influence of a DC-bias voltage indicate that there is a time related cap drift which can be much larger than the normal aging effect (Ref 1 and 2)
- So, if in application, the capacitors are exposed to a DC-bias voltage for a long time, the knowledge of the VCC and aging effects alone is not sufficient to predict the evolution of the capacitance of a capacitor over the course of its lifetime
- We decided to study this phenomenon



From "Ceramic Capacitor Aging: What to Expect"
ceramic-capacitor-aging-what-to-expect.pdf

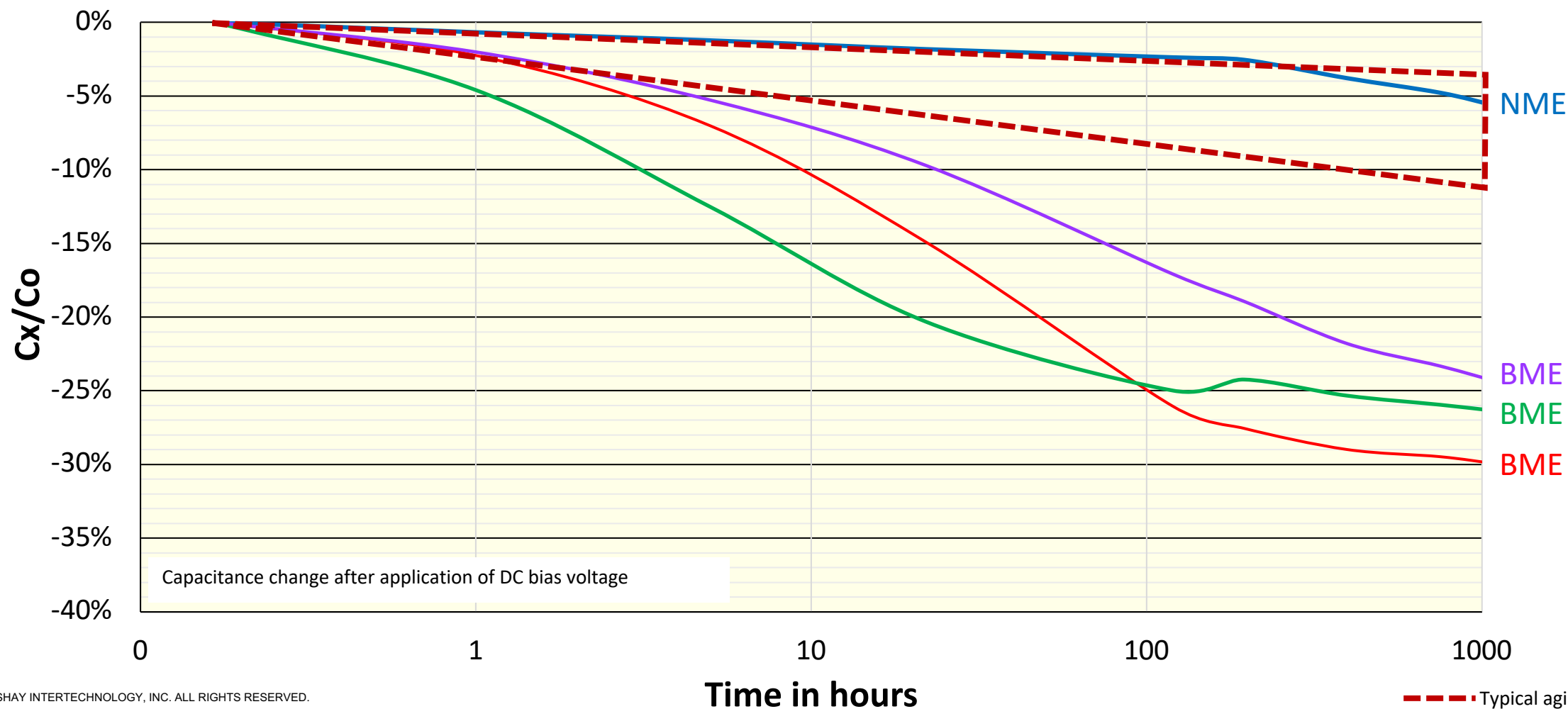
Test Setup and Procedure

- Ten (10) capacitors were mounted on a PCB and subjected to a constant DC-bias voltage over the entire duration of the test
- One group of parts was manufactured with noble metal electrodes while the three other group were base metal technology
- This test was done at 2 voltage levels and also at elevated temperature
 - 40 % Rated Voltage, 25 °C
 - 100 % Rated Voltage, 25 °C
 - 40 % Rated Voltage, 80 °C
- At defined periods of time, the parts were temporarily removed from their fixture and cap-tested at the same DC-bias voltage
 - When testing was performed at higher temperature, the parts were cooled to room temperature before cap measurements were made
- For the evaluation of the recovery behavior of the capacitors after long exposure to bias voltage, the terminals of parts were constantly shorted to prevent the build-up of any remaining voltage
- Complete de-aging was performed at 150 °C for a duration of 1 h



Exposure to 40 % of Rated Voltage at Room Temperature

- Capacitance change of a 50 V 0603 100nF MLCC over time with 20 V bias constantly applied at 25 °C

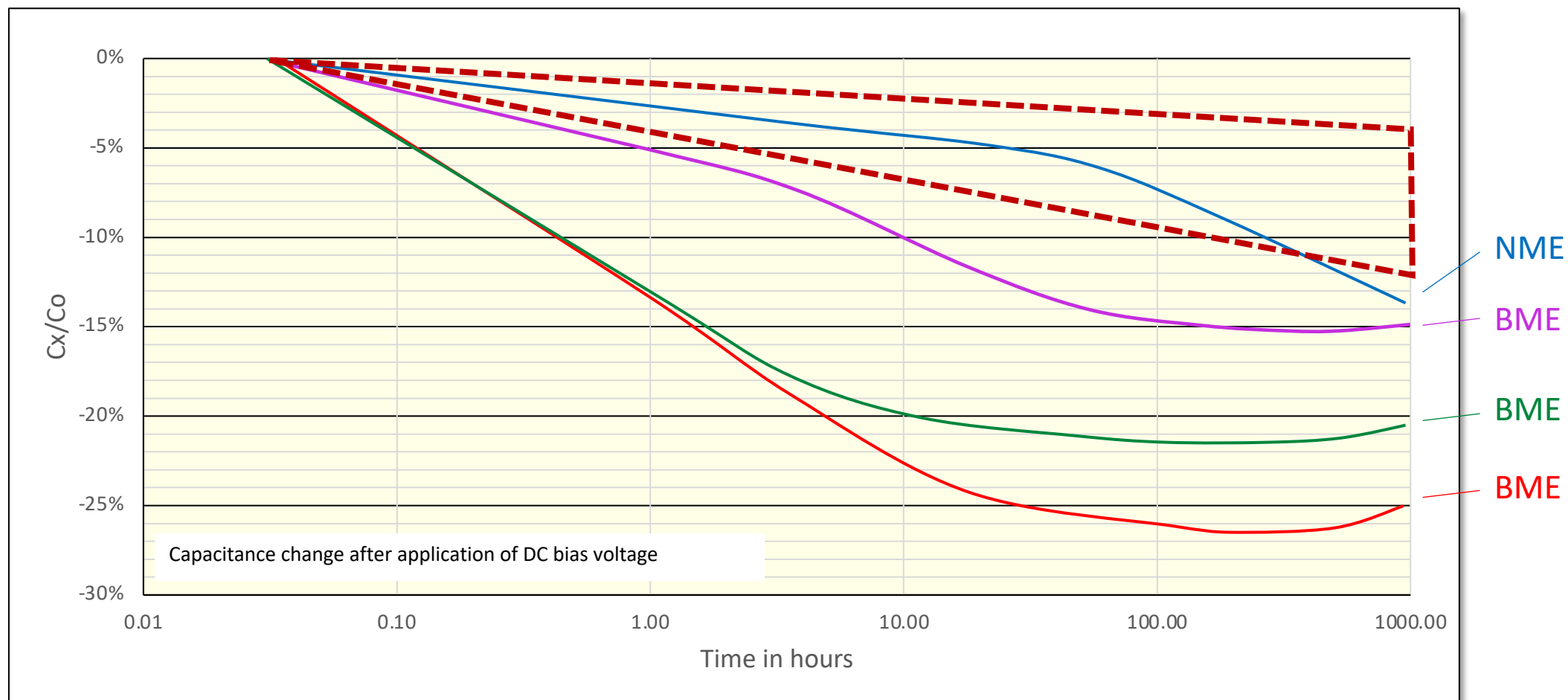


Exposure to 40 % of Rated Voltage at Room Temperature

- Observations
 - BME capacitors show much more cap drift under the influence of DC-bias than would be expected due to normal bias and aging estimates
 - After 1000 hours, loss was between 24 % and 30 %
 - NME capacitors drift was far less than the drift exhibited by the BME capacitors
 - The drift observed for the NME capacitors was in line with the typical 1 % to 3 % / decade aging drift
 - NME capacitors exhibit higher remaining capacitance after longer exposure time than BME capacitors

Exposure to 100 % of Rated Voltage at Room Temperature

- Capacitance change of a 50 V 0603 100nF MLCC over time with 50 V bias constantly applied at 25 °C

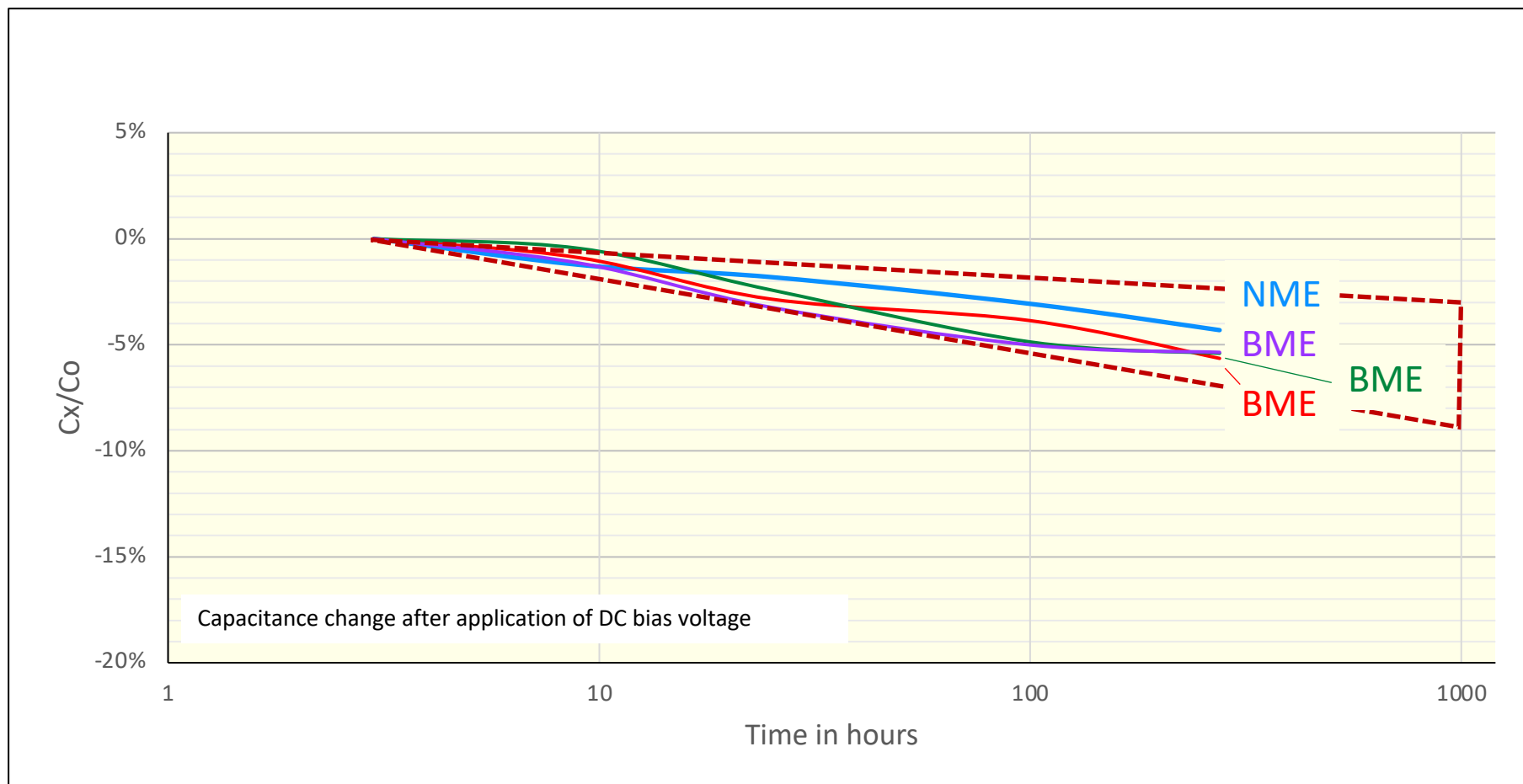


Exposure to 100 % of Rated Voltage at Room Temperature

- Observations
 - All capacitors exhibited drift greater than what would be expected from aging drift alone.
 - As would be expected, when exposed to the full rated voltage, the capacitance drift proceeds at a much higher speed, though it ends up at a similar point
 - NME capacitors drift was still less than the drift exhibited by the BME capacitors, though not as significantly as what occurred at 40% of rated voltage.
 - The BME capacitors showed a wider range of loss, between 15 % and 25 %
 - The conclusions are valid for DC-bias fields in the order of 6 V/ μm and higher

Exposure to 40 % of Rated Voltage at Elevated Temperature

- Capacitance change of a 50 V 0603 100 nF MLCC over time with 20 V bias constantly applied at 80 °C

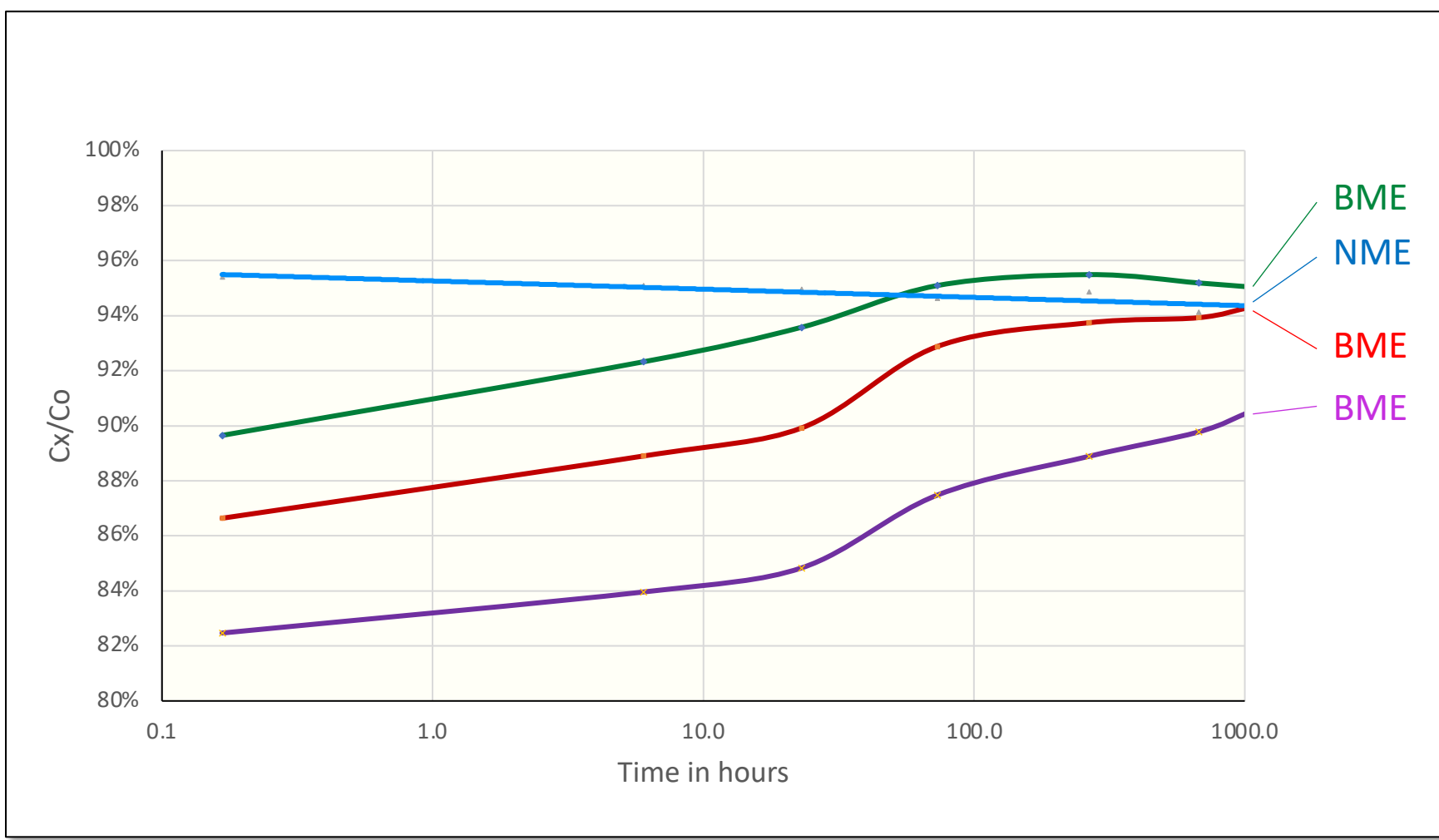


Exposure to 40 % of Rated Voltage at Elevated Temperature

- Observations
 - At elevated temperature, the BME losses were still slightly more than the NME losses, but the difference was much smaller
 - Perhaps the temperature coefficient of capacitance dominates the cap loss

Recovery After Long Bias Exposure

- Capacitance recovery (zero bias) in 0603 X7R 100 nF, 50 V MLCC following 1000 h of exposure to 50 V bias



Recovery After Long Bias Exposure

- Observations
 - When the DC-bias voltage is removed, the capacitors do recover at room temperature. However:
 - The NME capacitors recovered very quickly to 95 % of the original value in just a few minutes
 - The BME capacitors took much longer to recover – from 50 to 1000 h to reach 95 % recovery
 - After treatment at 150 °C for 1 h, all capacitors returned to their initial values
 - This suggests that the drift due to the bias voltage is related to time dependent changes in the domain structure as a result of prolonged exposure to a bias field

Conclusions and Recommendations

- Confirming reports from the field, there does appear to be a capacitance drift of Class 2 MLCCs due to long-term DC bias exposure
- The drift seems to be more severe in base metal electrode products than in noble metal electrode products
- At high temperature, the difference in drift between electrode systems seems to be less
- Recovery after the voltage is removed also varies; NME parts recover almost instantaneously while BME part can take up to 1000 to recover
- Deaging the parts (raising the temperature above the Curie point) reverses the loss, suggesting this is a phenomenon related to changes in the domains structure
- If the application is sensitive to capacitance value, this drift should be accounted for during the circuit design

More Information and References

- See the full study, “Time-Dependent Capacitance Drift of X7R MLCCs Under Exposure to a Constant DC Bias Voltage”, [HERE](#).

References

1. Effects of MgO Doping on DC Bias Aging Behavior of Mn-Doped BaTiO₃, Dong Woo HAHN et AlI, Japanese Journal of Applied Physics Vol. 47, No. 7, 2008, pp. 5526–5529
2. Mechanism of capacitance aging under DC-bias field in X7R-MLCCs, Takaaki Tsurumi et AlI, J. Electroceram (2008) 21:17–21

White Paper

Multilayer Chip Capacitors

Time-Dependent Capacitance Drift of X7R MLCCs Under Exposure to a Constant DC Bias Voltage

A Comparative Case Study on 0603 X7R 100 nF, 50 V MLCCs (Vishay and Three Competitors)

By Paul Coppens, El Bershadsky, John Rogers, and Brian Ward

ABSTRACT
Until recently, it was assumed that multilayer ceramic capacitor (MLCC) manufacturers' data stating the typical voltage coefficient of capacitance (VCC) and the maximum bias voltage were sufficient to predict the behavior of capacitance under DC bias aging. This paper reports on a comparative case study of capacitance drift of reported X7R MLCCs under DC bias aging. The results show that the capacitance drift of X7R MLCCs under DC bias aging is significantly higher than what is reported in the manufacturers' data. The results also show that the capacitance drift of X7R MLCCs under DC bias aging is significantly higher than what is reported in the manufacturers' data.

THE VCC EFFECT EXPLAINED
In class II dielectrics, the spontaneous polarization of the ceramic and the associated development of domains is responsible for the initial high capacitance. If the polarization is shifted as a function of the applied field, as in Fig. 1, a hysteresis loop is formed. The area of the loop is proportional to the VCC. The VCC is high, but it is not constant. The VCC is a function of the applied field and the aging time.

AGING PHENOMENA IN FERROELECTRIC CERAMICS
Above the Curie temperature, barium titanate exhibits a cubic structure. In this state the dielectric is not ferroelectric, and no spontaneous polarization is observed. Upon cooling down below the Curie temperature, the crystal structure changes to tetragonal. This allows the titanium atom to permanently move off-center in the crystal lattice, giving rise to a permanent polarization. Over time, the domains re-arrange continually, reducing internal strain. This slow re-arrangement of domains causes the capacitance to decrease over time. Typically, aging follows a logarithmic law whose mathematical expression is described as:

$$C_t = C_0 \left(1 - \frac{A}{100} \log_{10} t \right)$$

where:
C = capacitance after time t
C₀ = initial capacitance
A = aging constant

THE DC BIAS AGING TEST SETUP AND PROCEDURE
10 0603 X7R 100 nF, 50 V rated capacitor samples from Vishay and three other MLCC manufacturers were mounted on printed circuit boards (PCB). Complete de-aging was performed on all capacitors at 150 °C for a duration of 1 hour prior to testing. These capacitors on PCBs were inserted into a fixture and subjected to a constant DC bias voltage of 40 % and 100 % rated voltage over the entire duration of the test. After defined periods of time, the PCBs were temporarily removed from their fixtures with parts still holding most of their electrical charge. Capacitance was then measured while applying the same test voltage level and polarity. PCBs were then returned to their fixtures to continue DC bias aging up to 1000 hours.

LONG-TERM EXPOSURE TO 100 % RATED VOLTAGE AT ROOM TEMPERATURE
On a second set of samples, the capacitors were subjected to 100 % of rated voltage (50 V_{DC}). The interest here was to see how DC bias aging is affected by a higher field. Fig. 6 shows the capacitance loss over time, again referenced from the capacitance after 50 V bias applied. Comparing Fig. 5's loss with 40 % bias, and Fig. 6's loss with 100 % bias, the plot of Fig. 6 shows that capacitance loss proceeds at a faster rate. Competing capacitors initially showed much more capacitance drift under the influence of DC bias than Vishay capacitors, which again remained more stable up to 100 hours. However, this advantage was gradually lost at around 1000 hours of bias exposure.



Relative Capacitance Change Over Time in 0603 X7R 100 nF, 50 V MLCC With 50 V Bias Applied



SUMMARY
LONG-TERM EXPOSURE TO 40 % RATED VOLTAGE AT ROOM TEMPERATURE
Prolonged exposure of X7R capacitors to a DC bias voltage led to a capacitance decrease that was much stronger than the natural drift due to aging. Competing capacitors experienced much more capacitance drift under the influence of DC bias than Vishay's device, which remained more stable up to 1000 hours. Due to their low capacitance drift under the influence of DC bias voltage, Vishay capacitors have the highest remaining capacitance after longer exposure time. The conclusions are valid for DC bias fields in the order of up to 2.5 V/μm. Since MLCCs are seldom used at 100 % rated voltage, this voltage stress condition is applicable to the majority of the MLCCs in the field.

LONG-TERM EXPOSURE TO 100 % RATED VOLTAGE AT ROOM TEMPERATURE
As in the case of exposure to DC bias at 40 % of rated voltage, prolonged exposure of X7R capacitors to a DC bias voltage leads to a relatively strong capacitance drift. Exposed to the full rated voltage, the capacitance drift proceeds at a much higher rate. Competing capacitors initially showed much more capacitance drift under the influence of DC bias than Vishay's capacitor, which remained more stable up to 100 hours. Vishay's advantage gradually diminished around 1000 hours of exposure. The conclusions are valid for DC bias fields in the order of 6 V/μm and higher.

RECOVERY RATES
When the DC bias voltage was removed, competing capacitors recovered much more slowly than Vishay's device, which saw a 95 % capacitance recovery in just a few minutes after bias was removed. Competing capacitors took between 50 hours and 1000 hours or more to reach 95 % recovery. All tested capacitors recovered to 100 % after thermal treatment at 150 °C for 1 hour.

CONCLUSIONS
Vishay's introductory testing of the effects of DC bias aging on class II MLCCs supports prior reports. The Vishay capacitor tested proved to be the least affected by DC bias aging, as it had the smallest capacitance drift over time. This study was not an investigation into the physical, chemical, or material reasons for differences in performance between MLCC manufacturers. However, the complete recovery of the capacitance after heating above the Curie temperature seems to indicate that DC bias aging is related to time-dependent changes in the domain structure resulting from prolonged exposure to a bias field. Also, Vishay MLCCs are produced using noble metal technology. The three competing parts tested were made using base metal technology. These material differences could be a factor explaining the contrast in aging behavior observed. It is now clear that capacitance loss vs. DC bias aging is a critical characteristic that engineers need to know during design evaluation. In response, Vishay is beginning DC bias aging tests on our X7R dielectric systems to provide this data. Vishay's DC bias aging tests will be conducted for at least 100 hours or greater, with 20 %, 40 %, and 60 % of the rated voltage applied at room temperature.

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[6] Mechanism of Capacitance Aging Under DC Bias Field in X7R-MLCCs, Takaaki Tsurumi et al, J. Electroceram (2008) 21:17-21