TIME DEPENDENT CAPACITANCE DRIFT OF X7R MLCCS UNDER EXPOSURE TO A CONSTANT DC-BIAS VOLTAGE

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CMSE 2024

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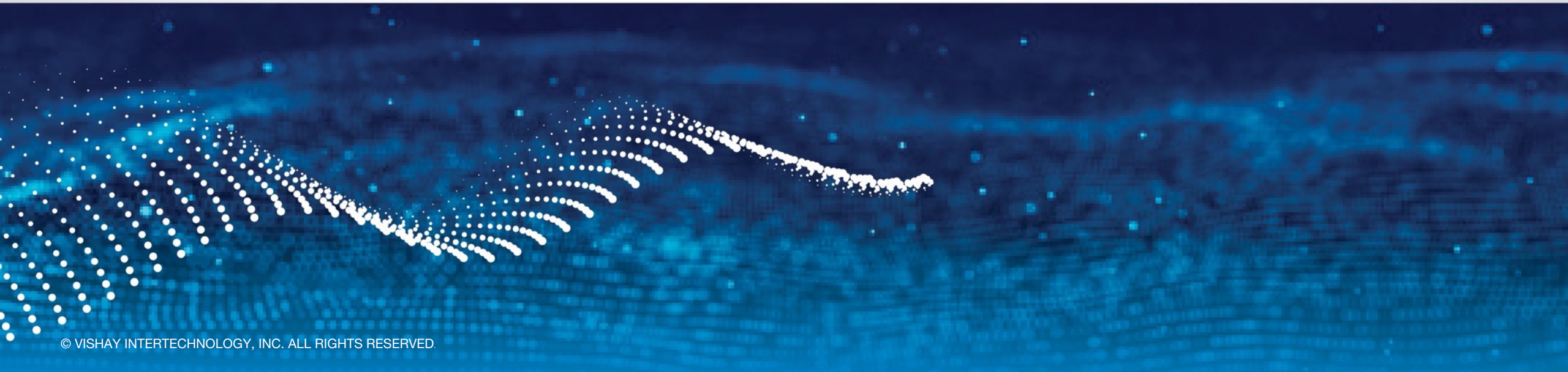


Time Dependent Capacitance Drift of X7R MLCCs Under Exposure to a Constant DC-Bias Voltage

- Abstract: Until recently, it was assumed that multilayer ceramic capacitor (MLCC) manufacturers' data stating the typical voltage coefficient of capacitance (VCC) and capacitance loss due to aging (no bias) could be additive, and that further capacitance drift over time will not be significant. However, recent research of the capacitance changes of X7R MLCCs under exposure to a constant DC bias voltage has shown that a time-related capacitance drift exists that can be much larger than the typical VCC and normal aging effect combined. This was first questioned by an automotive manufacturer and reported as an issue in critical systems that was related to capacitance loss and bias aging. A study of the DC Bias aging for a very common MLCC (0603 X7R 100nF 50V) was performed which subjected the capacitors to DC bias at 40% and 100% of the rated voltage for more than 1000 hours. The capacitance was measured intermittently to measure the drift. Results indicated the construction and/or material system of the part affected the degree of capacitance drift. Recovery of the capacitance after the bias was removed, also tended to depend on this construction.

Background

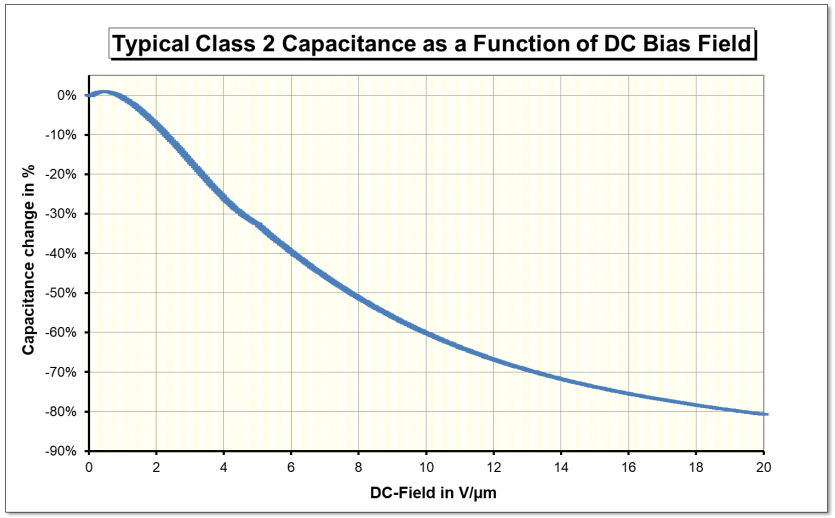
- Multilayer Ceramic Capacitors (MLCCs) offer advantages to the designer:
  - High capacitance, low ESR, low cost, and insensitivity to high temperature assembly
- MLCCs do exhibit changes of their electrical characteristics due to applied voltage and operating temperature, which depends on the nature of the dielectric material used

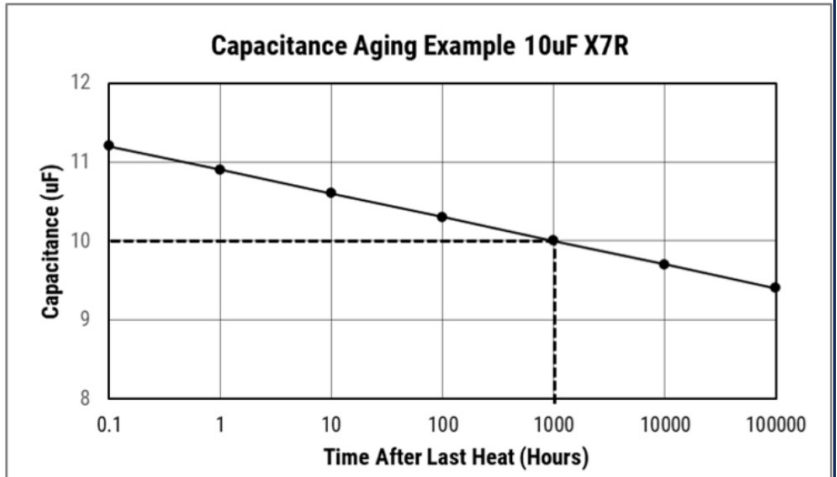
Class 1 (NP0/C0G)	Class 2 (X7R)
• Based on paraelectric ceramic + Stable, low loss dielectric material + Very limited effect of voltage and temperature. - Downside: lower dielectric constant → lower available capacitance for a given size	• Based on ferro-electric ceramic compositions. + Higher dielectric constant → higher capacitance values - Downside: capacitance is affected by operating environment

- Because of the high stability of the electrical characteristics and relatively low capacitance values, capacitors of Class 1 are not subject of this study
- However, several factors affect the stability of the electrical characteristics of Class 2:
  - Temperature, DC-bias voltage, frequency, AC-voltage amplitude as well as aging of capacitance and dissipation factor over time

Background

- Until recently, it was assumed that the loss of capacitance in Class 2 MLCCs was due to 3 factors:
  - Application of a DC-bias voltage
  - Aging of the capacitor
  - Temperature
- However, recent reports of the capacitance change over time under the influence of a DC-bias voltage indicate that there is a time related cap drift which can be much larger than the normal aging effect (Ref 1 and 2)
- So, if in application, the capacitors are exposed to a DC-bias voltage for a long time, the knowledge of the VCC and aging effects alone is not sufficient to predict the evolution of the capacitance of a capacitor over the course of its lifetime
- We decided to study this phenomenon

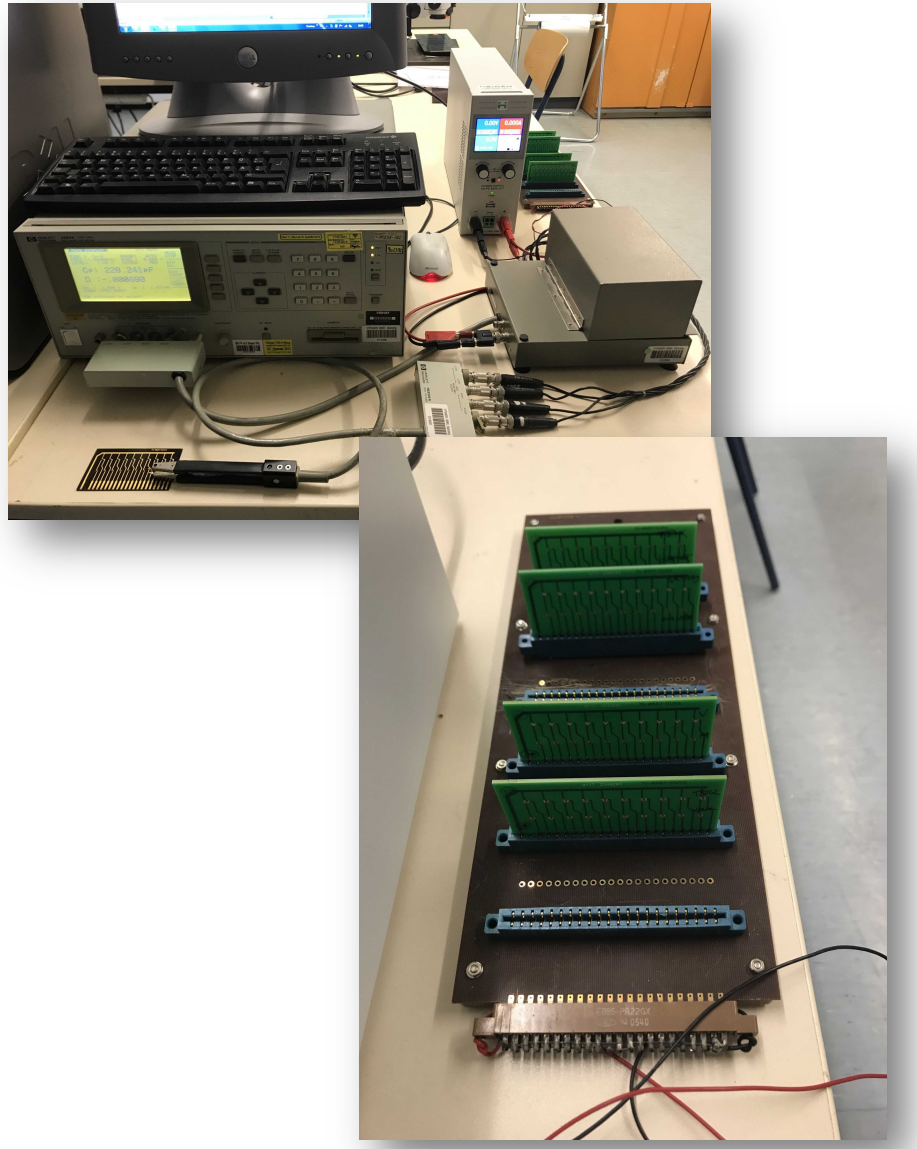




From “Ceramic Capacitor Aging: What to Expect”
ceramic-capacitor-aging-what-to-expect.pdf

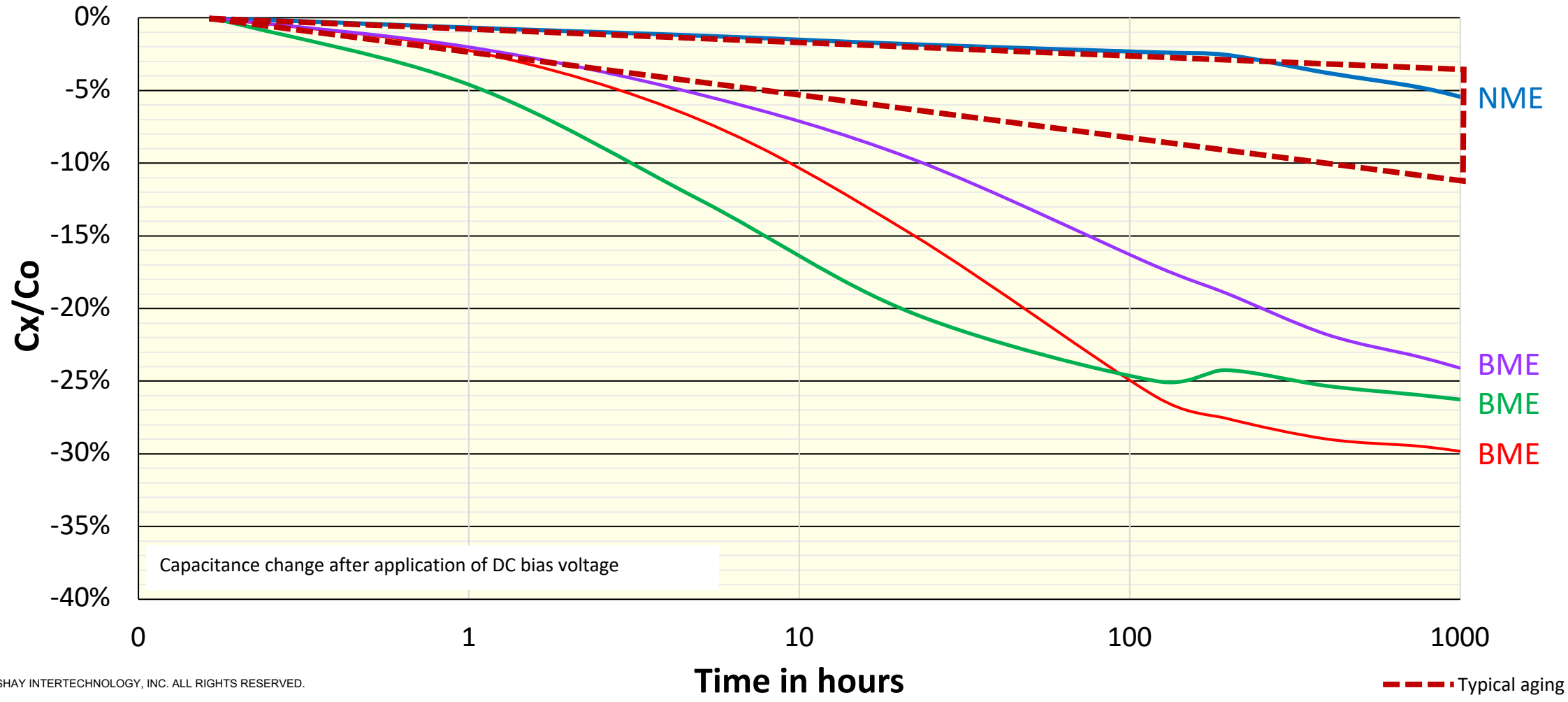
Test Setup and Procedure

- Ten (10) capacitors were mounted on a PCB and subjected to a constant DC-bias voltage over the entire duration of the test
- One group of parts was manufactured with noble metal electrodes while the three other group were base metal technology
- This test was done at 2 voltage levels and also at elevated temperature
  - 40 % Rated Voltage, 25 °C
  - 100 % Rated Voltage, 25 °C
  - 40 % Rated Voltage, 80 °C
- At defined periods of time, the parts were temporarily removed from their fixture and cap-tested at the same DC-bias voltage
  - When testing was performed at higher temperature, the parts were cooled to room temperature before cap measurements were made
- For the evaluation of the recovery behavior of the capacitors after long exposure to bias voltage, the terminals of parts were constantly shorted to prevent the build-up of any remaining voltage
- Complete de-aging was performed at 150 °C for a duration of 1 h



Exposure to 40 % of Rated Voltage at Room Temperature

- Capacitance change of a 50 V 0603 100nF MLCC over time with 20 V bias constantly applied at 25 °C

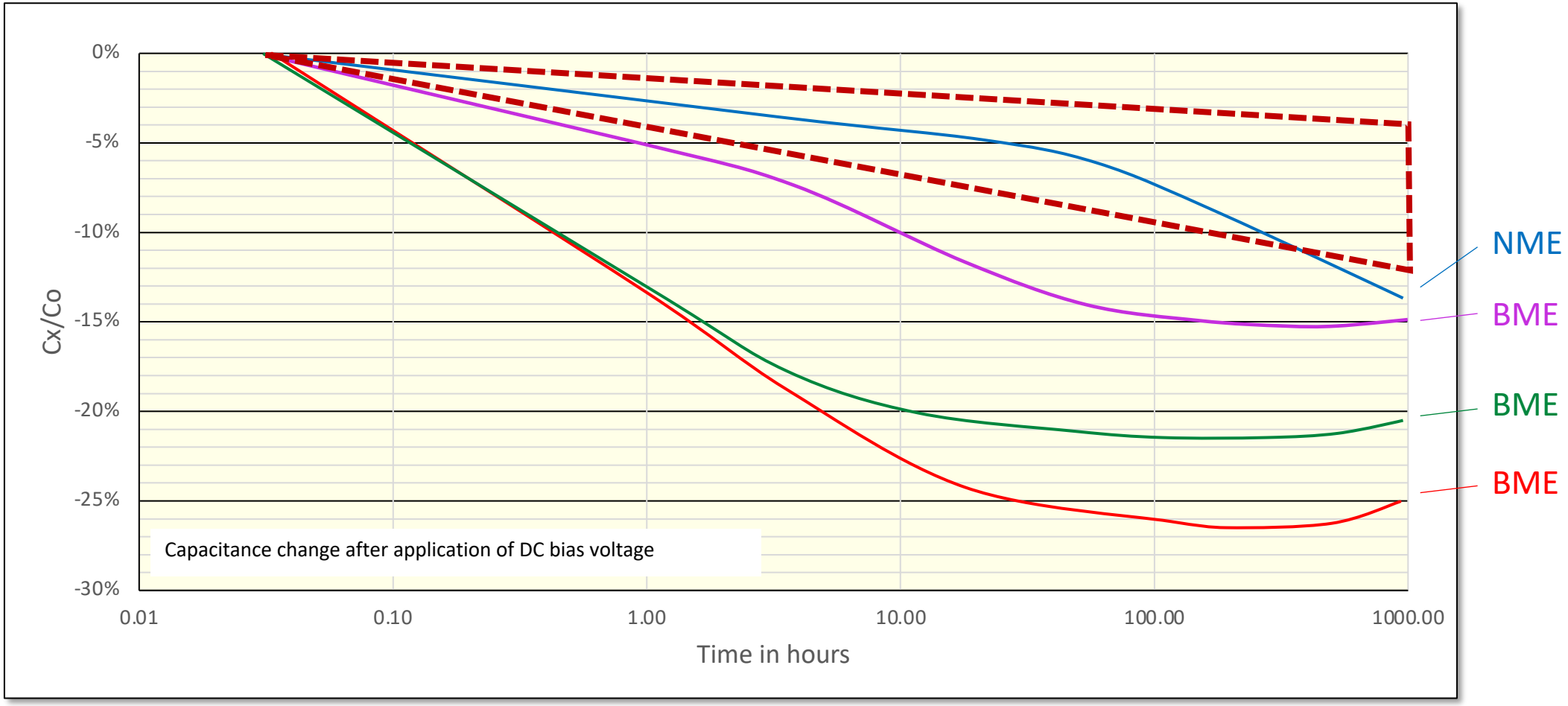


Exposure to 40 % of Rated Voltage at Room Temperature

- Observations
  - BME capacitors show much more cap drift under the influence of DC-bias than would be expected due to normal bias and aging estimates
    - After 1000 hours, loss was between 24 % and 30 %
  - NME capacitors drift was far less than the drift exhibited by the BME capacitors
    - The drift observed for the NME capacitors was in line with the typical 1 % to 3 % / decade aging drift
  - NME capacitors exhibit higher remaining capacitance after longer exposure time than BME capacitors

Exposure to 100 % of Rated Voltage at Room Temperature

- Capacitance change of a 50 V 0603 100nF MLCC over time with 50 V bias constantly applied at 25 °C

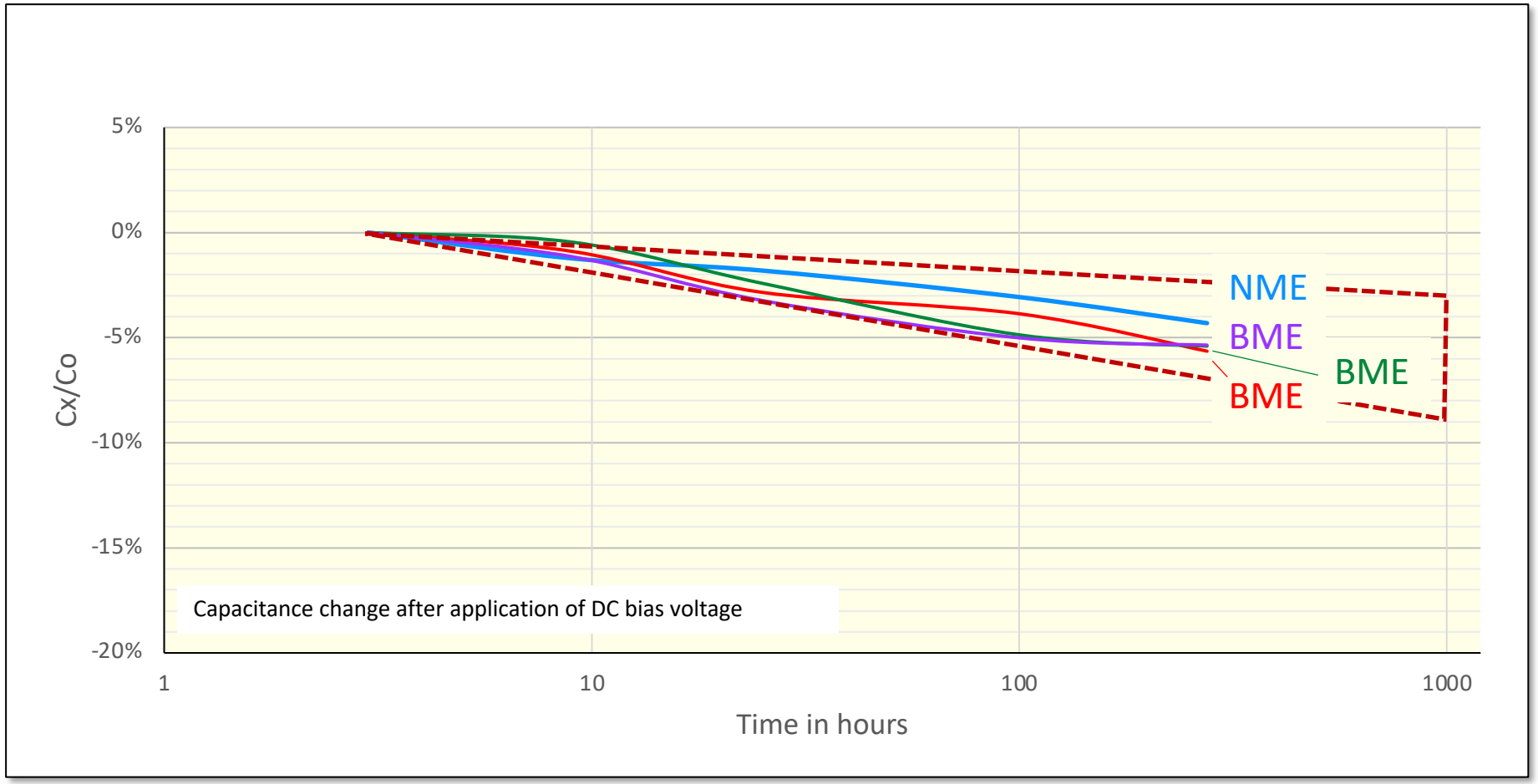


Exposure to 100 % of Rated Voltage at Room Temperature

- Observations
  - All capacitors exhibited drift greater than what would be expected from aging drift alone.
  - As would be expected, when exposed to the full rated voltage, the capacitance drift proceeds at a much higher speed, though it ends up at a similar point
  - NME capacitors drift was still less than the drift exhibited by the BME capacitors, though not as significantly as what occurred at 40% of rated voltage.
    - The BME capacitors showed a wider range of loss, between 15 % and 25 %
  - The conclusions are valid for DC-bias fields in the order of 6 V/µm and higher

Exposure to 40 % of Rated Voltage at Elevated Temperature

- Capacitance change of a 50 V 0603 100 nF MLCC over time with 20 V bias constantly applied at 80 °C

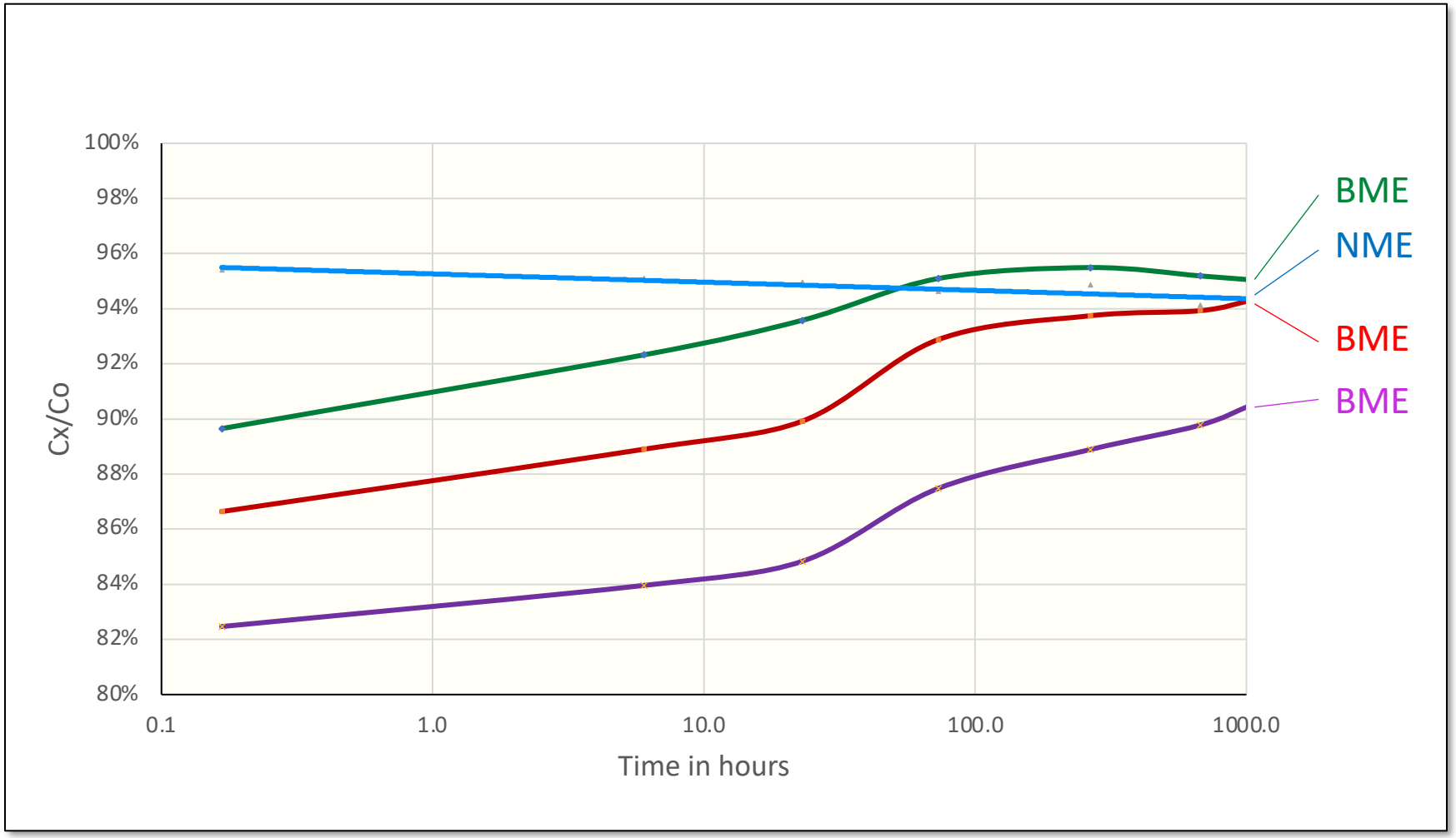


Exposure to 40 % of Rated Voltage at Elevated Temperature

- Observations
  - At elevated temperature, the BME losses were still slightly more than the NME losses, but the difference was much smaller
  - Perhaps the temperature coefficient of capacitance dominates the cap loss

Recovery After Long Bias Exposure

- Capacitance recovery (zero bias) in 0603 X7R 100 nF, 50 V MLCC following 1000 h of exposure to 50 V bias



Typical aging

Recovery After Long Bias Exposure

- Observations
  - When the DC-bias voltage is removed, the capacitors do recover at room temperature. However:
    - The NME capacitors recovered very quickly to 95 % of the original value in just a few minutes
    - The BME capacitors took much longer to recover – from 50 to 1000 h to reach 95 % recovery
  - After treatment at 150 °C for 1 h, all capacitors returned to their initial values
    - This suggests that the drift due to the bias voltage is related to time dependent changes in the domain structure as a result of prolonged exposure to a bias field

Conclusions and Recommendations

- Confirming reports from the field, there does appear to be a capacitance drift of Class 2 MLCCs due to long-term DC bias exposure
- The drift seems to be more severe in base metal electrode products than in noble metal electrode products
- At high temperature, the difference in drift between electrode systems seems to be less
- Recovery after the voltage is removed also varies; NME parts recover almost instantaneously while BME part can take up to 1000 to recover
- Deaging the parts (raising the temperature above the Curie point) reverses the loss, suggesting this is a phenomenon related to changes in the domains structure
- If the application is sensitive to capacitance value, this drift should be accounted for during the circuit design

More Information and References

- See the full study, “Time-Dependent Capacitance Drift of X7R MLCCs Under Exposure to a Constant DC Bias Voltage”, *HERE*.
- References

1. Effects of MgO Doping on DC Bias Aging Behavior of Mn-Doped BaTiO3, Dong Woo HAHN et All, Japanese Journal of Applied Physics Vol. 47, No. 7, 2008, pp. 5526–5529
2. Mechanism of capacitance aging under DC-bias field in X7R-MLCCs, Takaaki Tsurumi et All, J. Electroceram (2008) 21:17–21