VPT Component's Development of Radiation Hardened MOSFETs with LA Semiconductor

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Overview

- VPT Components has developed a family of radiation hardened silicon power MOSFETs in conjunction with LA Semiconductor (Pocatello, ID).
- The MOSFETs use a mature, flight proven design and are radiation hardened to 100krad(Si) total ionizing dose (TID).
- The MOSFETs are single event gate rupture (SEGR) and single event burnout (SEB) immune at full rated drain potential (100V) and zero gate potential using a 15MeV/n xenon (Xe) beam.
- VPT Components power MOSFETs are also resistant to SEGR and SEB using a 15MeV/n gold (Au) beam when used with a de-rated drain to source bias.

VPT Components Snapshot

- Second largest supplier of JAN devices by product count
- Business Established in 2007 as Hi Rel Components; Acquired by Aeroflex, Cobham and MACOM. Became VPT Components Sept 21st, 2018
- Fully consolidated completely refurbished state-of-the-art 50,000 sq ft facility in Lawrence, Massachusetts
- DLA certified to MIL-PRF-19500 and MIL-PRF-38535 with JANS diode line certified December 2009 and JANS and JANSR transistor/SCR line certified March 2012
- Laboratory Suitability Status MIL-STD-750 & MIL-STD-883 with over 90 test methods performed on site.

LA Semiconductor Site Overview – KEY STATS

Location: Pocatello, Idaho

- Campus: 33 acres with 545k ft^2 of building spaces
- 8-inch wafer fab built in 1997 with photo capability to 0.18 μm
- Current technologies: Digital & Analog CMOS, BCD, advanced discrete, MEMS, Trench PowerFET's, TSV, and custom technologies
- Capacity: 19k+ wafers/month with **room to expand to 32k wafers/month** (mix dependent)
- Class-1, Ballroom Cleanroom: 72k square feet
  - **+ 7k ft^2 convertible Annex fab space**
  - **+ 8k ft^2 unfinished Ballroom fab space**
- Certified to automotive IATF16949, military/aerospace AS9100, QML, ISO 14001, OHSAS 18001, and ISO 9001

Fab History

2005

American Microsystems became AMIS and went public in 2005. American Microsystems came to Pocatello in 1971.

2008

Onsemi acquired the AMIS fabs in Pocatello, Idaho. Most technologies are CMOS ASICs. Onsemi introduced Discrete products (circuit protection devices, power MOSFETs, etc.) into the Pocatello 8" line.

2022

LA Semiconductor LLC, with the purchase of the Pocatello site, established a US owned and operated pure-play foundry to provide dedicated on-shore wafer supply focused on linear, analog, and power products. LA Semiconductor will also continue to supply Onsemi for a minimum of 5 years.

LAS Fab-1 – Rad Hard Focus, On-shore operations

- ✔ Proven record of Rad Hard device performance (rad hard by design and rad hard by process)
- ✔ Only U.S. owned & operated Analog Power & Discrete fab – 100% on-shore operations
- ✔ Best-in-class quality & costs
- ✔ Innovative product roadmaps
- ✔ Process development in high volume production facility
- ✔ Auto, Medical & Trusted* certified
- ✔ Flexible support for small & mid-size customers

Technology Portfolio

Technology name	Tech subgroup	Tech type	Tech Description	Max VDD
	G8x	0.8um CMOS	0.8um gate with W-plug backend	5V
	G6x	0.6um CMOS	0.6um gate with low contact resistance	5V/20V
	G4x	0.35um CMOS	0.35um gate with Cobalt silicide module	3.3V/5V
	G2x	0.18um CMOS	In development	1.8V/3.3V/ 5V/12-80V
	G1x	0.13um CMOS	Beginning development	
	L6x	40V Bipolar	In development	

Foundry Pivot - Operations Plan

COMPREHENSIVE DESIGN SUPPORT ENVIRONMENT

Leverage highly efficient and capable manufacturing operations
Bring teams together to create a design environment, accelerating customer acquisition & project transfers
Invest in capability expansion to match demand

EDA TOOLS & SUPPORT

- ✔ Support all Major Vendors
- ✔ Maintain Close Collaboration
- ✔ Validate Design Flows
- ✔ Develop Dedicated Tools

PROCESS DESIGN KITS

- ✔ Develop & Release Models
- ✔ License Models Where Available
- ✔ Reference Design Flows
- ✔ Scalable Layout Cells (pcells)

MPW SHUTTEL PROGRAMS

- ✔ Low Cost
- ✔ Rapid Prototyping
- ✔ Full Manufacturing Environment
- ✔ Custom Processing Options

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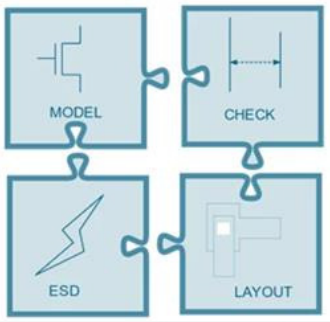
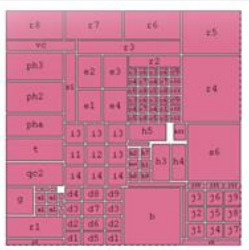
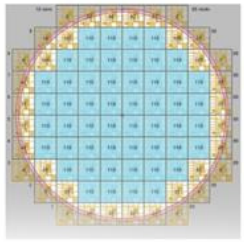






Capabilities: Certifications & Standards

LA SEMICONDUCTOR

Certifications

- Trusted Foundry Accreditation
- MIL-PRF-38535
- AS9100 Rev D. -Aviation, Space and Defense
- IATF 16949 -Automotive Standard
- ISO 14001 -Environmental Standard
- ISO 9001 -Quality Management Systems
- C-TPAT –Supply Chain Security

Reliability Standards

- JEDEC JEP001 Foundry Process Qualification
- JEDEC JESD47 Stress-Test-Driven Qualification of Integrated Circuits
- AEC-Q-100 Failure Mechanism Based Stress Tests Qualification for Integrated Circuits
- MIL-PRF-38535L General Specification for Integrated Circuits (Microcircuits) Manufacturing
- Compliant to ISO/IEC 17025 and ANSI/NCSL Z540 accredited calibration standards

RadHard MOSFET Development

- The RadHard MOSFET development was targeted to be similar to “R5” generation power MOSFETs made by Aeroflex RAD from 2010 – 2016 at Micrel.
- These MOSFETs offer proven reliability and low on-resistance with millions of device hours of flight heritage. One basic design makes 100V-250V parts in Size 1, 3 and 6.
- These devices are fabricated at LA Semiconductor in Pocatello, ID
- The first part developed was a Size 3 100V MOSFET in 2023
- The goal was to be TID hardened to 100krad(Si) and SEGR/SEB immune to full rated drain potential using Xe (LET~60MeV-cm2/mg & 15MeV/n beam)
- The devices passed Au (LET~80MeV-cm2/mg & 15MeV/n beam) with a de-rated VDS of no more than 40% (i.e. 60V).

Key Features of the RAD7130 MOSFET

- The RAD7130 is similar to the 2N7481 (MIL-PRF-19500 / 703) and has fully passed to the /703 Slash Sheet.
- BVDSS=100V, RDSon ≤ 50mΩ (package dependent)
- 22A Continuous Current in a medium sized die (~125mils x ~180mils)
- The MOSFETs were built using a custom fabrication process at LA Semi using their radiation hardened gate oxide.
- The RAD7130 was built on 8” wafers with 0.0018-0.0022 Ω-cm substrates and a special p+ epitaxial layer designed to make these devices hardened to single event burnout (SEB) and single event gate rupture (SEGR).

RAD7130 MOSFET Die Specifications

Die Size

- 126mils ± 2mils x 182mils ± 2mils

Gate Pad

- 11 mils ± 1mil x 0.23 ± 1.5mils

Die Thickness

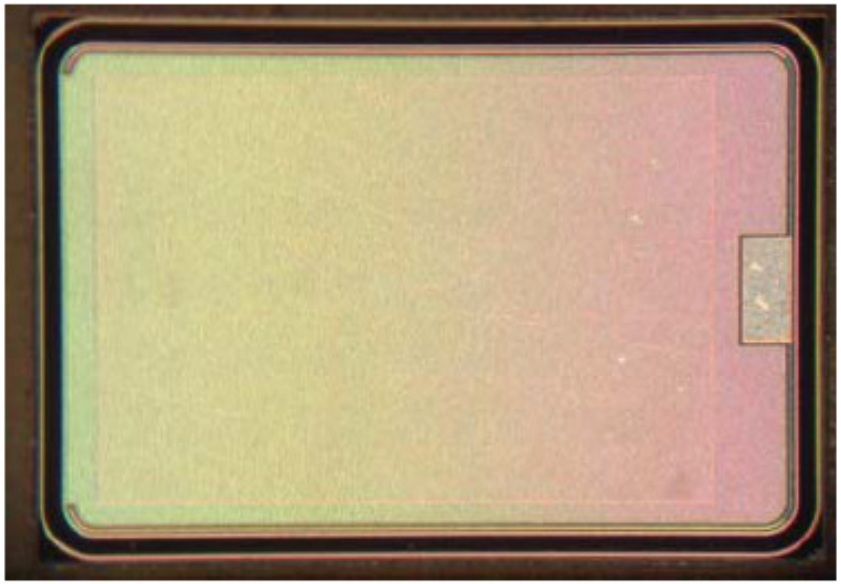
- 14 mils ± 1mil

Top Metal

- 40kA (±10%) Al 1% Si

Back Metal

- Ti(2kA)NiV(10kA)Ag(2kA) (±10%)

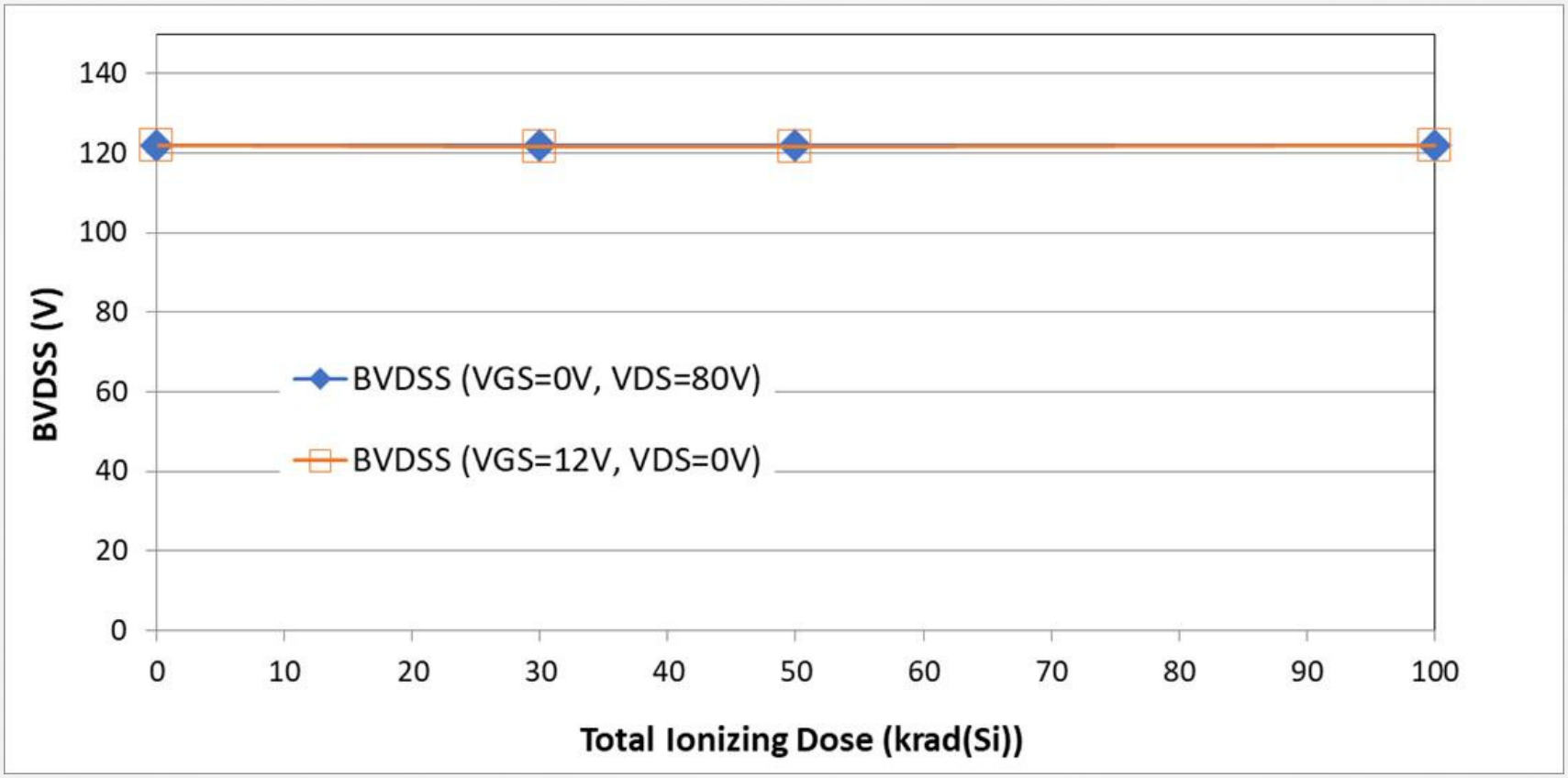


RAD7130 MOSFET TID Results

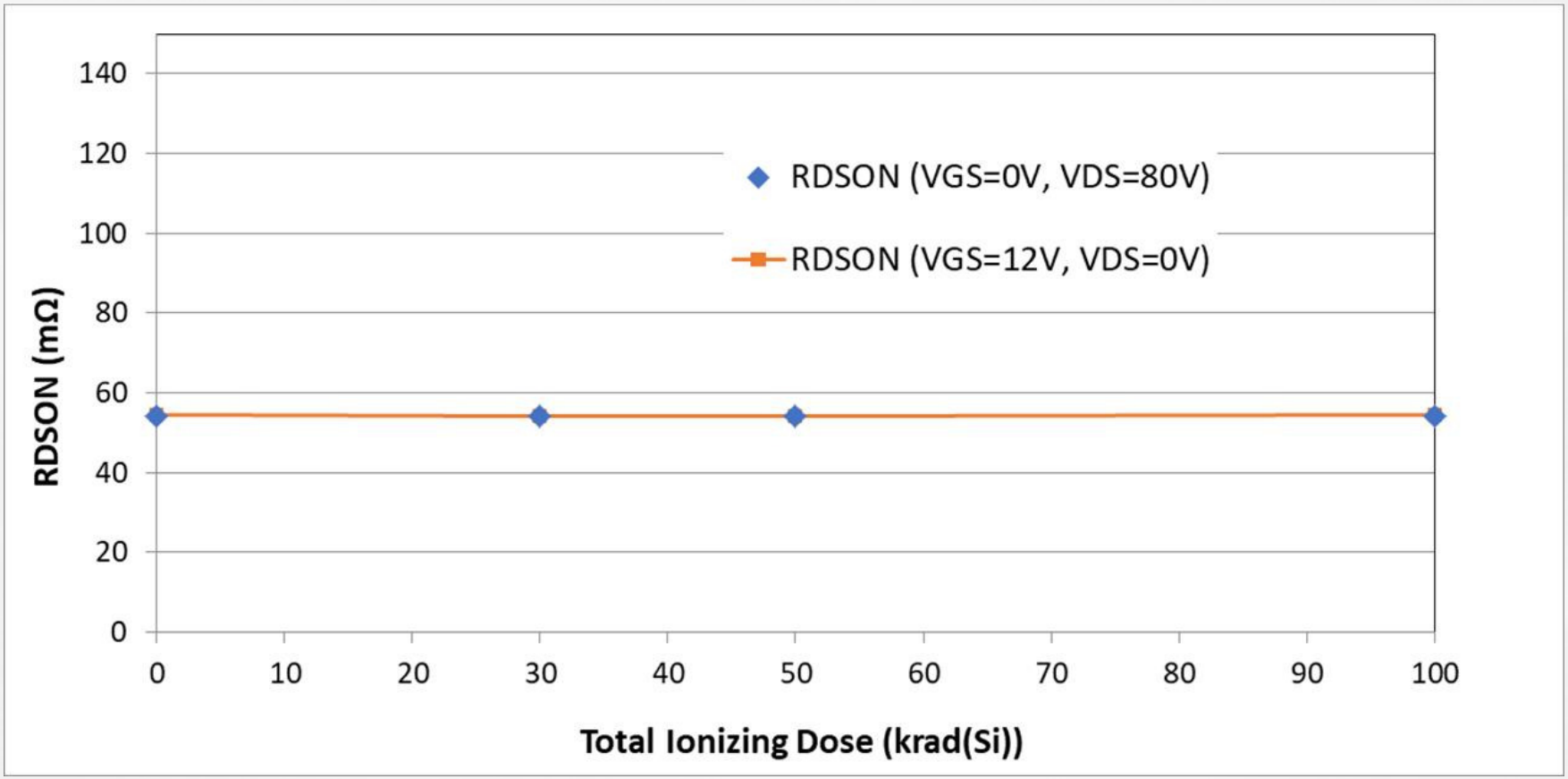
VPT COMPONENTS

Test Name	PRE	30k	50k	100k
IGSS F (A) @ VSG=20V	PASS	PASS	PASS	PASS
IGSS R (A) @ VSG=20V	PASS	PASS	PASS	PASS
IDSS1 (A) @ VDS=120V	PASS	PASS	PASS	PASS
IDSS2 (A) @ VDS=80V	PASS	PASS	PASS	PASS
BVDSS (V) @ ID=0.001A VMAX=500V	PASS	PASS	PASS	PASS
VTH1 (V) @ IG=0.001A	PASS	PASS	PASS	PASS
VTH2 (V) @ IG=0.001A	PASS	PASS	PASS	PASS
RDON (R) @ ID=17.6A VG=12V	PASS	PASS	PASS	PASS
VSD (V) @ ID=22A	PASS	PASS	PASS	PASS

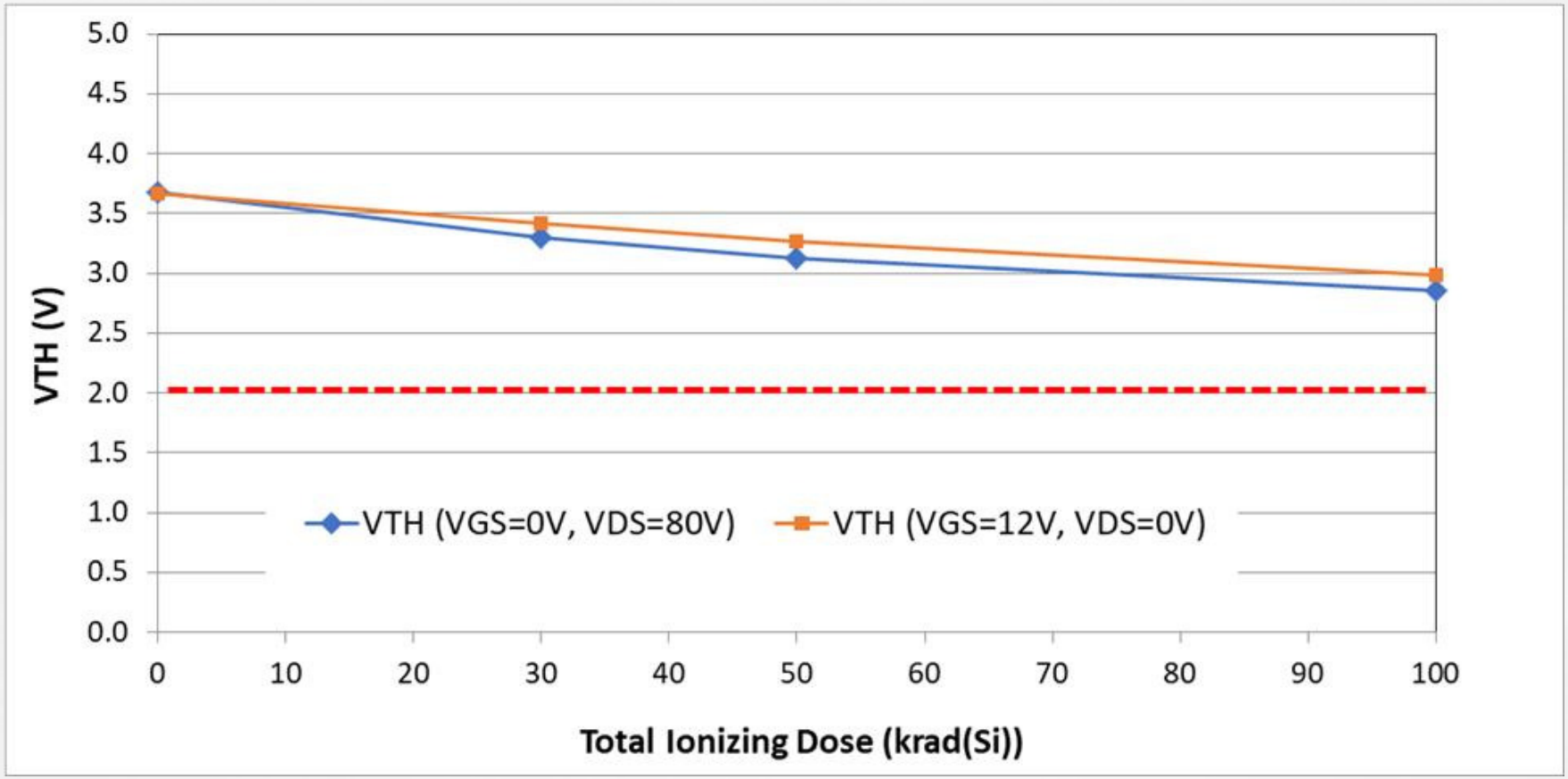
RAD7130 TID Results (BVDSS)



RAD7130 TID Results (RDSON)



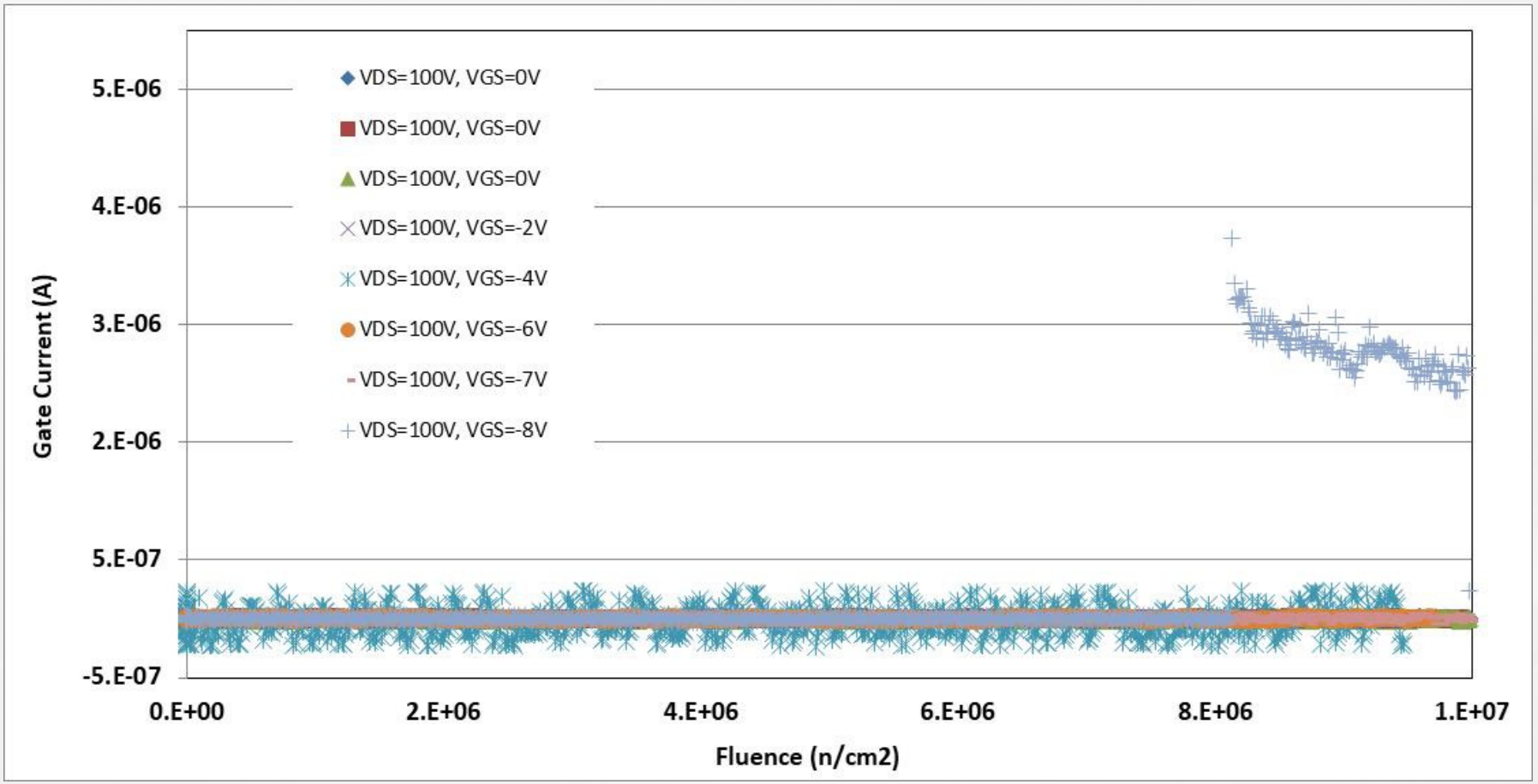
RAD7130 TID Results (VTH)



RAD7130 SEGR / SEB Data Log

Wafer Lot	DUT SN#	RUN	ION	Nominal LET (MeV-cm^2/mg)	Nominal range (µm)	Effective Total fluence (ions/cm^2)	Average flux (ions/(cm^{2}s))	DUT tilt angle (deg)
J79959	4	1	Xe	60	>100	9.96E+06	1.17E+05	0
J79959	5	2	Xe	60	>100	1.00E+07	1.19E+05	0
J79959	6	3	Xe	60	>100	9.99E+06	1.17E+05	0
J79959	7	4	Xe	60	>100	9.96E+06	1.16E+05	0
J79959	8	5	Xe	60	>100	1.00E+07	1.17E+05	0
J79959	8	6	Xe	60	>100	1.00E+07	1.16E+05	0
J79959	9	7	Xe	60	>100	1.00E+07	1.18E+05	0
J79959	9	8	Xe	60	>100	1.00E+07	1.21E+05	0
J79959	10	9	Xe	60	>100	9.99E+06	1.22E+05	0
J79959	10	10	Xe	60	>100	1.00E+07	1.21E+05	0
J79959	10	11	Xe	60	>100	1.00E+07	1.18E+05	0
J79959	11	12	Xe	60	>100	1.00E+07	1.28E+05	0
J79959	11	13	Xe	60	>100	9.96E+06	1.21E+05	0
J79959	11	14	Xe	60	>100	9.99E+06	1.22E+05	0
J82518	1	89	Xe	60	>100	1.00E+07	5.27E+04	0
J82518	2	90	Xe	60	>100	1.00E+07	5.18E+04	0
J82518	3	91	Xe	60	>100	9.99E+06	5.07E+04	0
J82518	4	92	Xe	60	>100	9.96E+06	5.33E+04	0
J82518	5	93	Xe	60	>100	9.98E+06	5.25E+04	0
J82518	6	94	Xe	60	>100	9.98E+06	5.23E+04	0
J82518	7	95	Xe	60	>100	9.99E+06	4.95E+04	0
J82518	8	96	Xe	60	>100	1.00E+07	4.61E+04	0

RAD7130 Gate Current vs Fluence



Post Heavy Ion Gate Stress Test Example:

SN#	Lot #	PRE/ POST	ION	RUN	IGSSF Max	IGSSR Max		PRE/ POST	IGSSF Max	IGSSR Max	Run Condition	Pass/ Fail
1	J82518	PRE	Xe	89	4.65E-09	-5.24E-09		POST	5.30E-09	-5.89E-09	VDS=100V, VGS=0V	Pass
2	J82518	PRE	Xe	90	6.88E-09	-7.82E-09		POST	6.72E-09	-7.36E-09	VDS=100V, VGS=0V	Pass
3	J82518	PRE	Xe	91	6.49E-09	-7.48E-09		POST	5.50E-09	-5.85E-09	VDS=100V, VGS=0V	Pass
4	J82518	PRE	Xe	92	5.35E-09	-6.00E-09		POST	7.87E-09	-8.16E-09	VDS=100V, VGS=-2V	Pass
5	J82518	PRE	Xe	93	4.76E-09	-2.61E-09		POST	6.41E-09	-2.77E-09	VDS=100V, VGS=-4V	Pass
6	J82518	PRE	Xe	94	5.04E-09	-5.83E-09		POST	5.94E-09	-6.12E-09	VDS=100V, VGS=-6V	Pass
7	J82518	PRE	Xe	95	6.02E-09	-6.79E-09		POST	2.13E-02	-1.73E-02	VDS=100V, VGS=-8V	FAIL
8	J82518	PRE	Xe	96	5.56E-09	-6.38E-09		POST	5.62E-09	-5.88E-09	VDS=100V, VGS=-7V	Pass

Summary/Conclusions

1. LA Semiconductor is long standing 8” wafer fab in Pocatello, ID with a wide variety of technologies and processes PLUS the flexibility to design custom flows for the High-Reliability market segment.
2. We developed a custom radhard process flow at LA Semi and used that flow to build a radhard “R5” generation Power MOSFET
3. The Power MOSFET passed 100krad(Si) TID and ~60MeV-cm2/mg Xe (15MeV/n) beam at full rated VDS with no SEB/SEGR
4. The TID radiation hardness was achieved using a custom radox flow applicable to higher voltage products.
5. SEE hardness was achieved using a specially designed P+ epitaxial layer (designed and fabricated by LA Semi) to minimize RDSOn while withstanding SEB/SEGR.