The Santa Clara Valley (Silicon Valley) Chapters:

Heterogeneous Integration (HI) Reliability

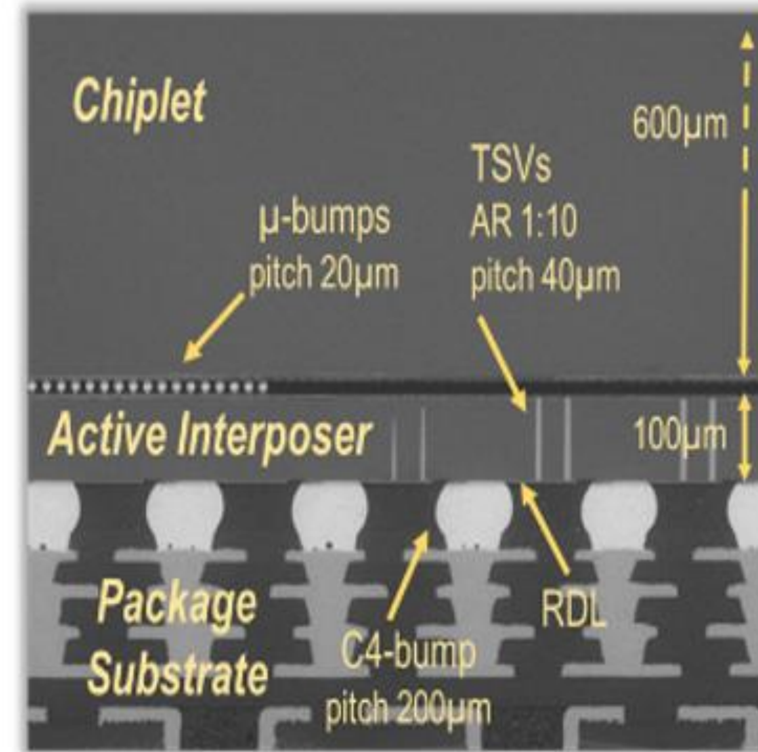
IEEE HIR Reliability TWG

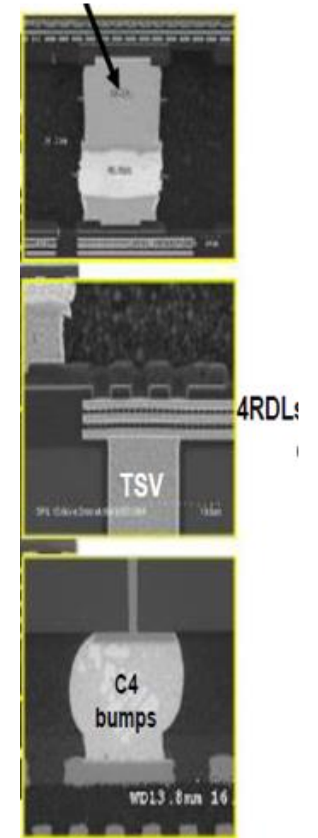
CPI and Design for CPI Reliability

- Chip to Package Interaction (CPI) Robustness and Reliability
  - Problem Statement of CPI Issues
  - CPI Failure Modes and Mechanisms
  - CPI Key Factors and Challenges
  - Design for CPI Robustness/Reliability
    - CPI Test Vehicle and Structures
    - CPI Qual Tests
    - CPI Simulations
    - CPI Design Rules

What is Chip to Package Interaction (CPI)?

- Any failure modes due to the mutual interaction between chip and package
  - Chip failures due to thermal mechanical stress from package
    - Corner cracking
    - Die edge cracking
    - Die bump cracking
    - UBM cracking
    - **Under bump/bond pad ELK cracking**
    - Die backside cracking
  - Package failures due to thermal mechanical stress from chip
    - Underfill cracking
    - Substrate failures
    - Bump cracking near substrate
  - Stress induced transistor performance shift
    - Overall package induced global stress
    - Bump/u-bump and TSV transmitted local stress





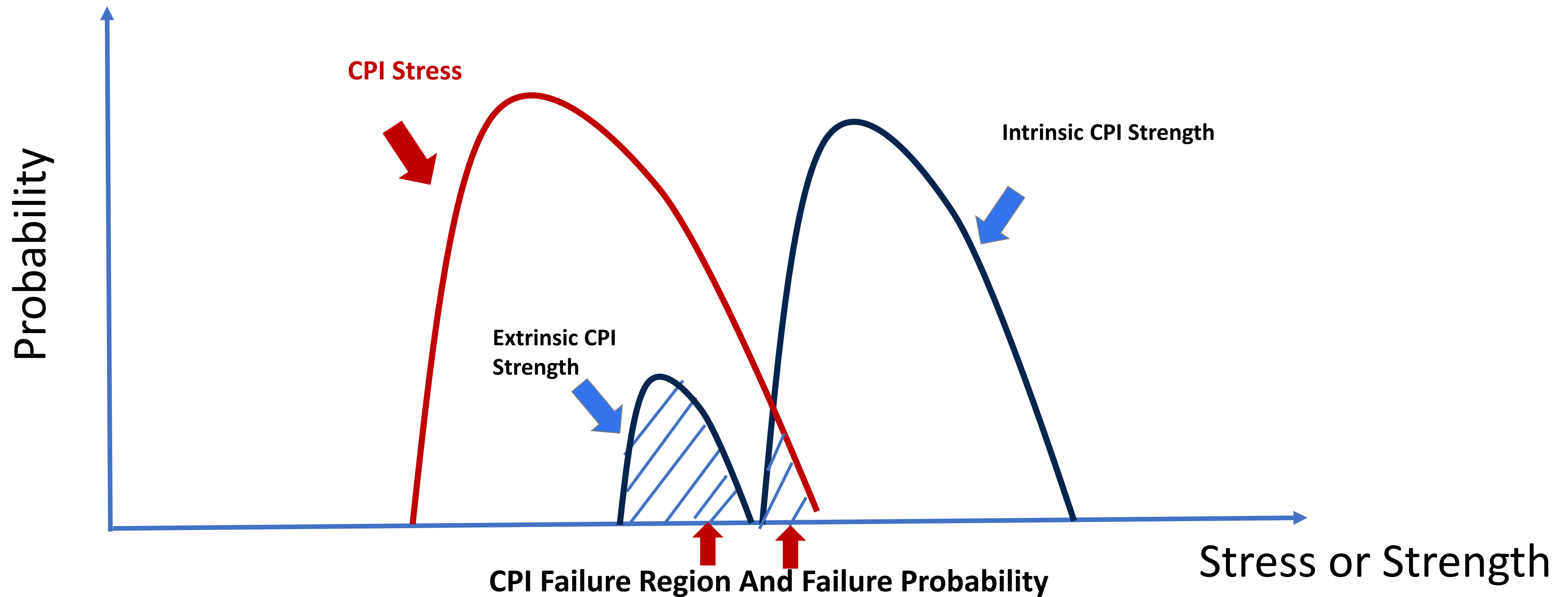
A Bit History About CPI

- Chip to Package Interaction (CPI) Happened
  - First introduction of low k at 0.13um (130 nm)
    - Cu wire bonding
  - Introduction of ELK
  - Pb free bumping
  - Cu pillar bumping
  - Round vs Oblong bumps
  - Thin core or coreless substrate
  - > 28Gb/s signal bumps
  - Full reticle size die
  - Adv packages ??

- Industry Activities
  - IRPS (Int Reliability Physics Symposium)
    - CPI Technical Committee
  - IEEE EPS (Electronics Packaging Society) Reliability Tech Committee
  - ECTC Applied Reliability Committee
  - IEEE REPP (Rel on Electronics and Photonics Packaging)
  - IITC (Intl Interconnect Tech Conf)
  - IEEE Heterogenous Integration Reliability Roadmap
  - IEEE IRDS (Intl Roadmap for Devices and System)

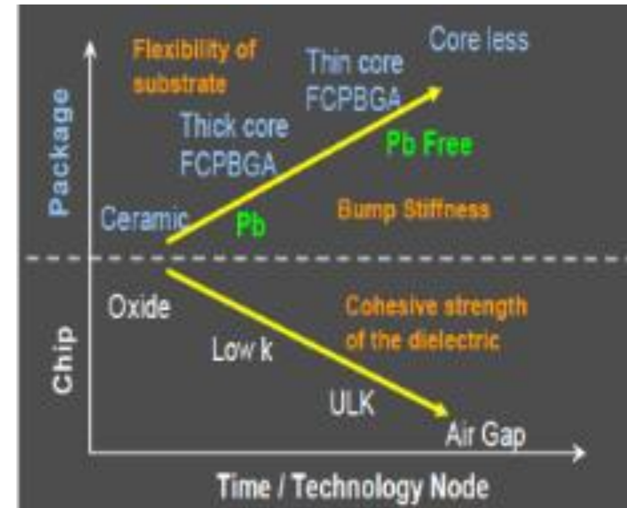
CPI Strength vs. CPI Stress

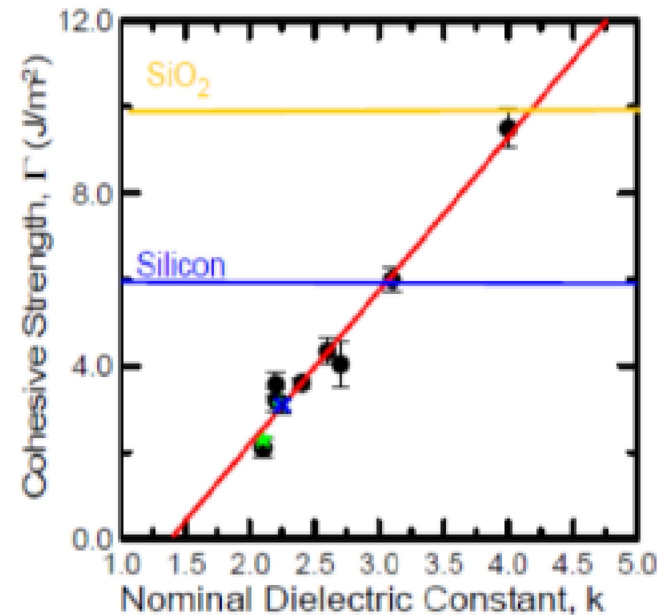
- CPI failure occurs when stress exceeds strength
- Both stress and strength are not fixed, they are in statistical distribution



Why is ELK Cracking Becoming More Prevalent?

- Low k and ELK/ULK introduction
  - Fragile and poor adhesion
- High speed pins
  - Constraints of metal filling
- Pb free or Cu pillar interconnect
  - Higher modulus
  - Transmit more stress to Si
- Large die size

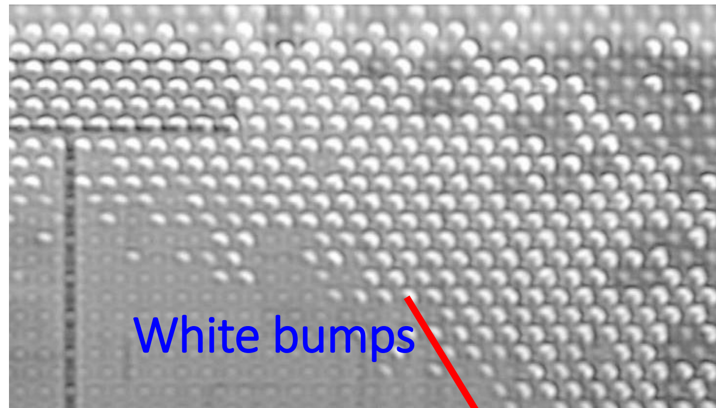


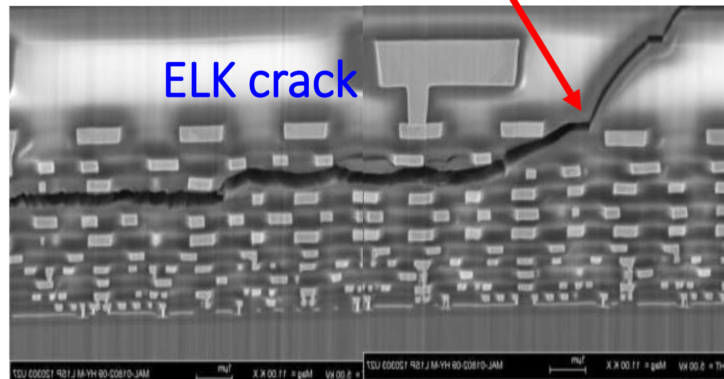


Typical CPI Induced Failures

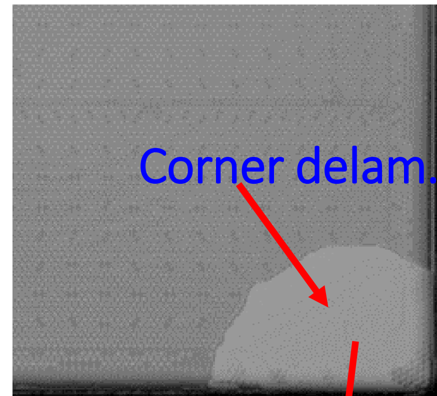
Stress Controlled

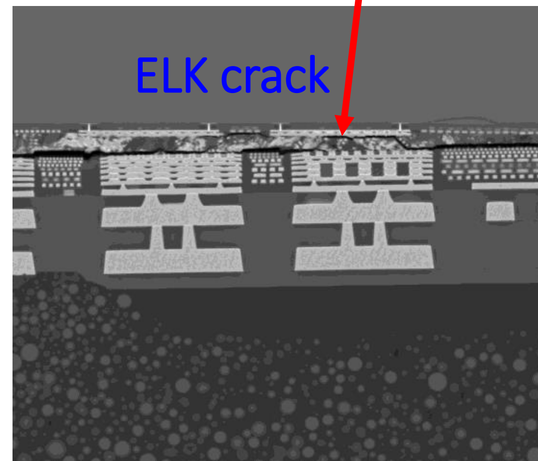
Under bump ELK cracking



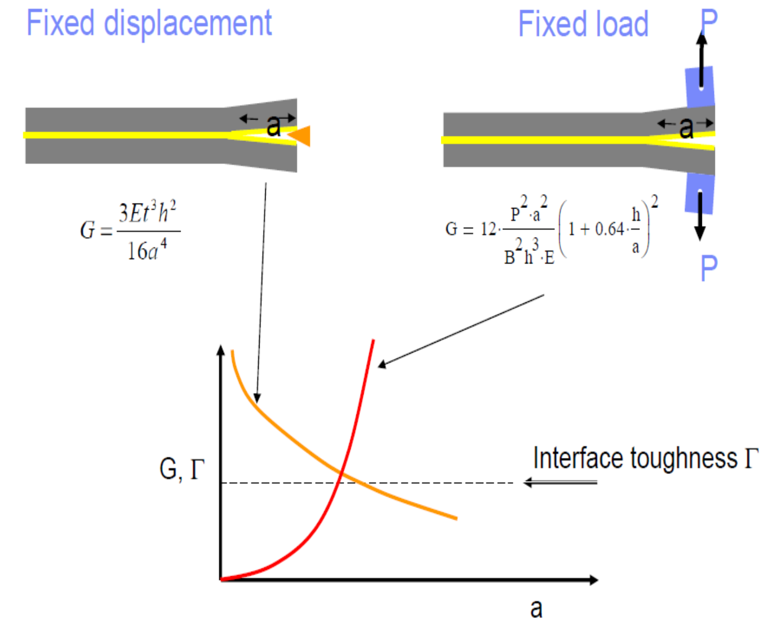


Die corner ELK cracking





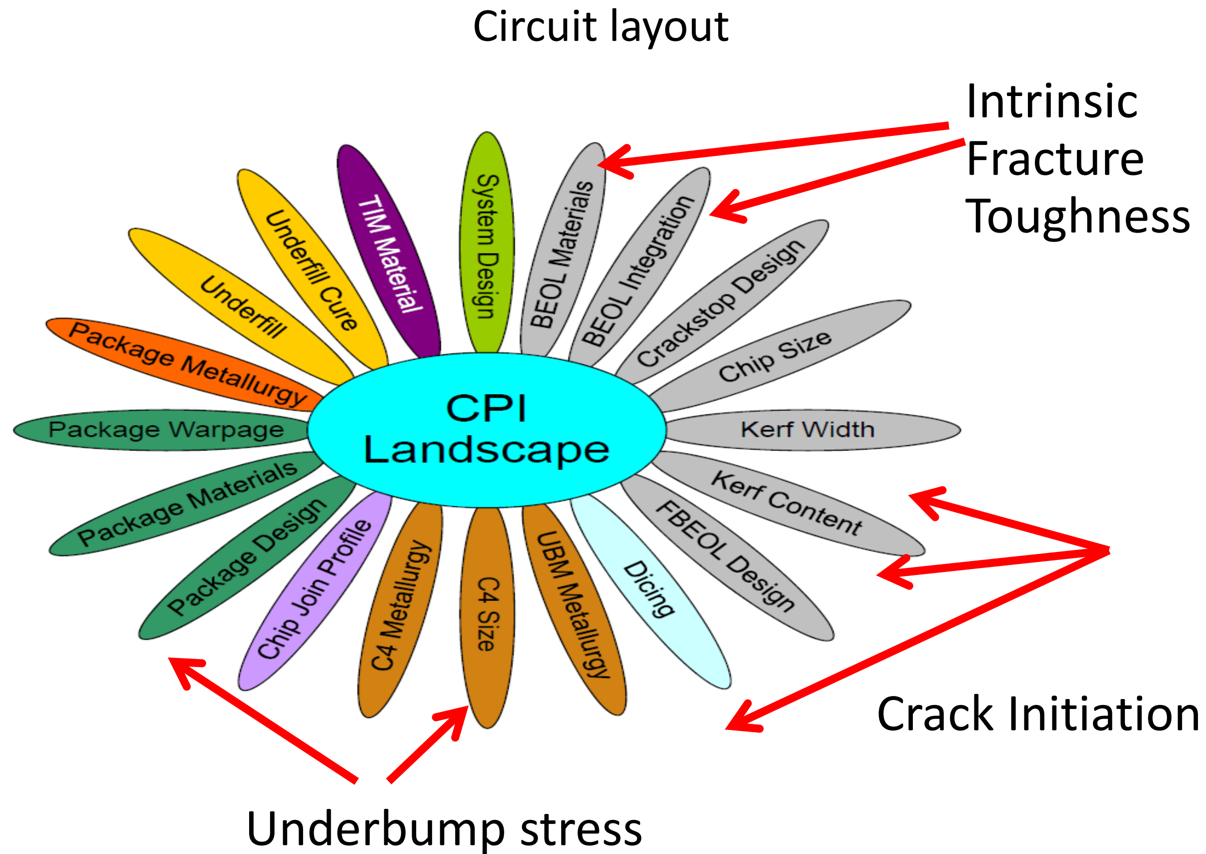
Displacement Controlled



Source: IBM

CPI Landscape

- (Thermo-) Mechanical stress during assembly processes
- Thermo-mechanical stress within the field application under environmental conditions
  - Isotropic hardening effect of solder material
  - CPI stress increases with thermal cycles
- Many variables difficult to control for a Silicon foundry



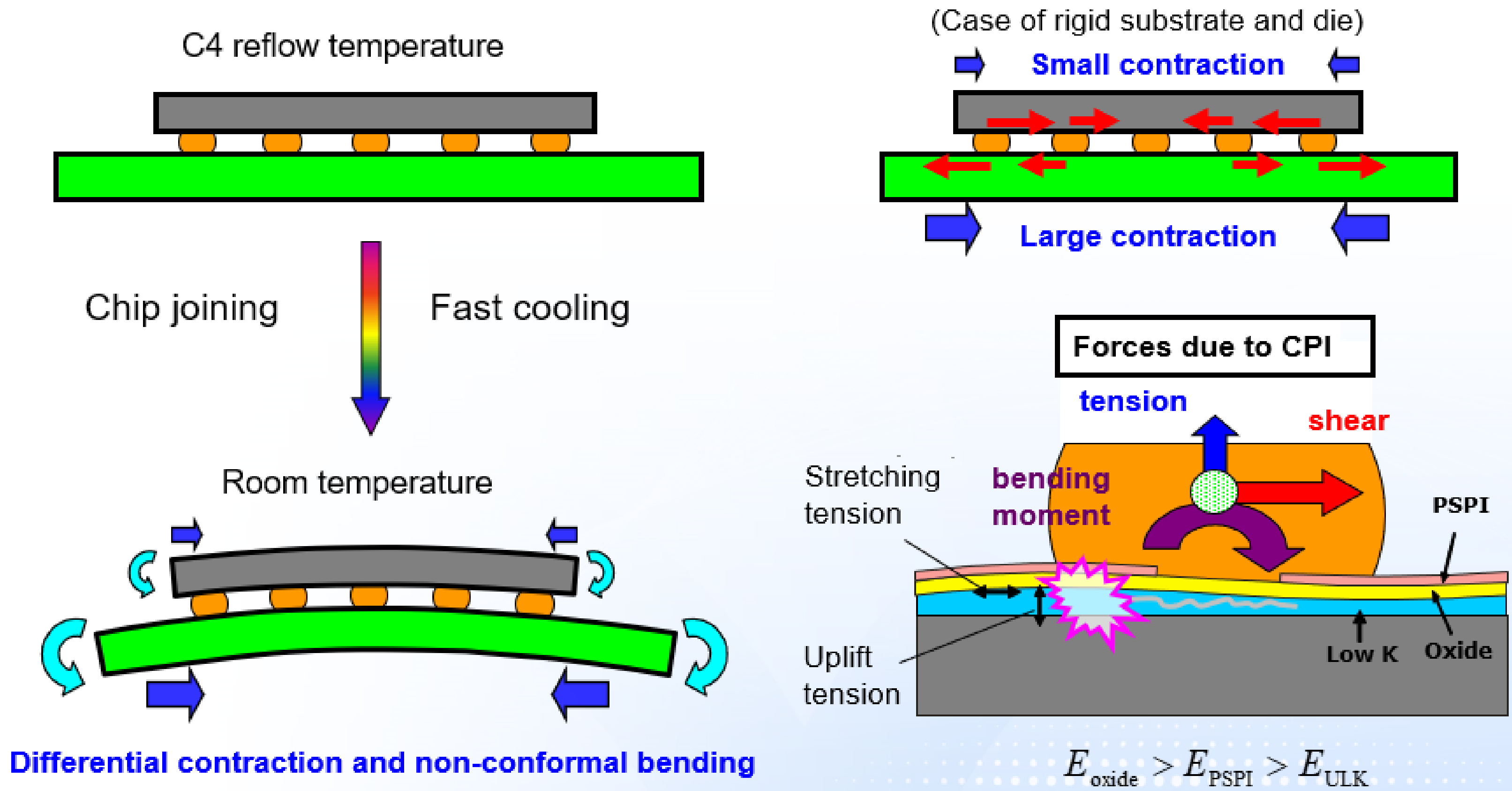
Source: IBM

Major Factors on Under Bump CPI Robustness and Reliability

- Materials
  - Substrate core CTE
  - Low k/ELK die
  - Pb free solder and Cu pillar bumps
  - Substrate pre solder material
- Design
  - Polyimide and opening size
  - UBM shape and orientation
  - Metal density and density gradient
  - Bump density
  - Die size
- Fab and Assembly Process
  - Fab process variations and defects in BEOL
  - Wafer dicing parameters
  - Flip Chip attachment profile

Under bump/bond pad LK/ELK cracking was an issue since the introduction of low k at 0.13um and still a challenging problem for 5nm!

Under Bump CPI Failure Mechanism



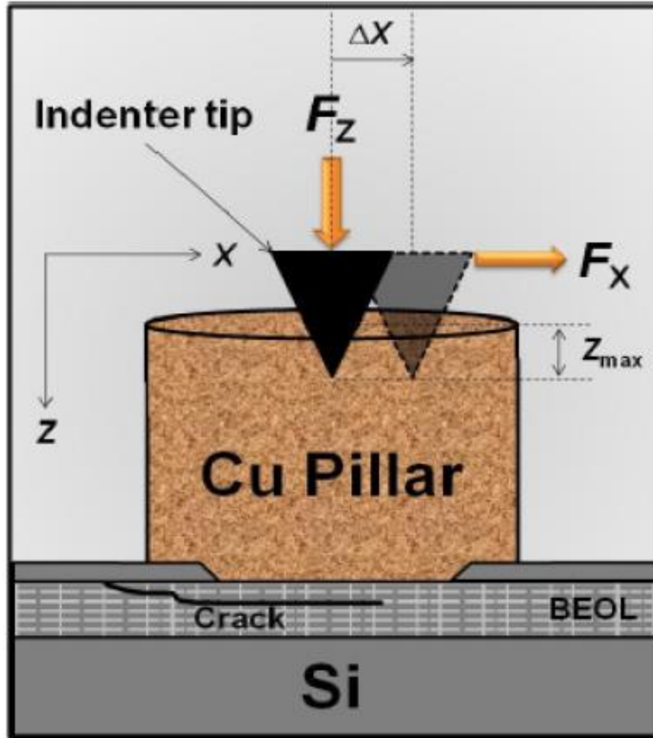
- Stress arises due to CTE mismatch between the substrate and the die.
- Substrate, C4 and BEOL are all involved in generating stress to cause ELK cracking.

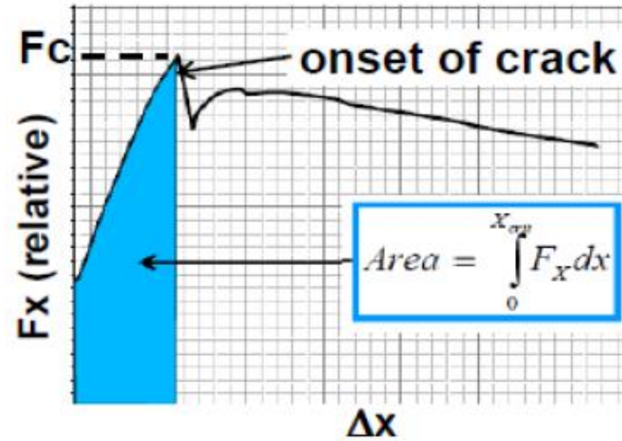
Source: IRPS 2016

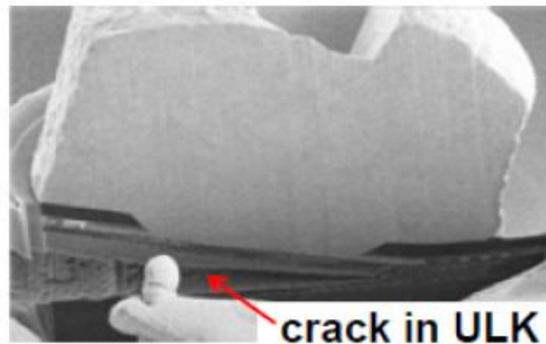
Source: Tom Shaw, IBM

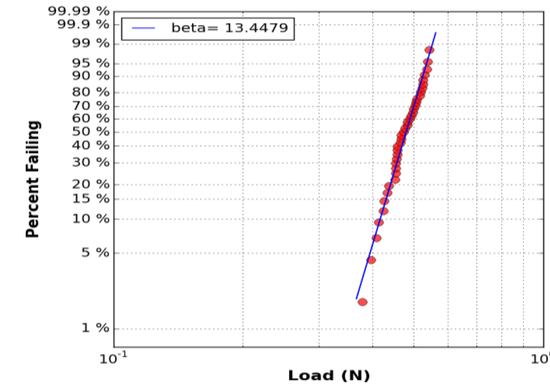
Under Bump CPI Strength Test

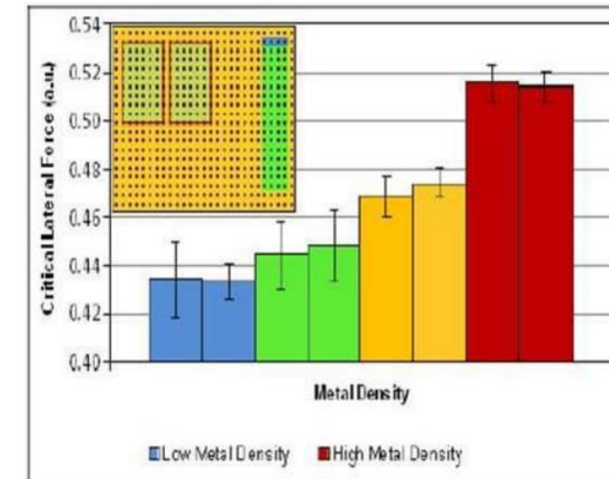
- To replicate the stress conditions and failure modes during flip chip assembly





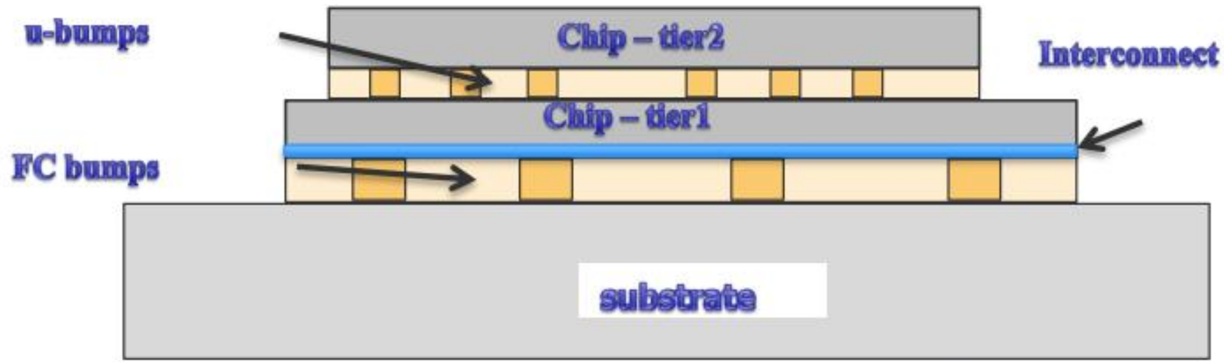


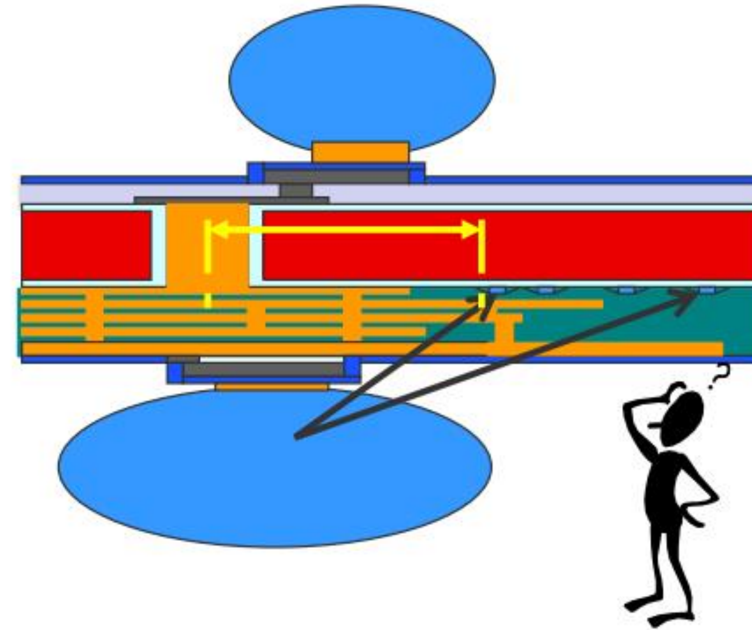




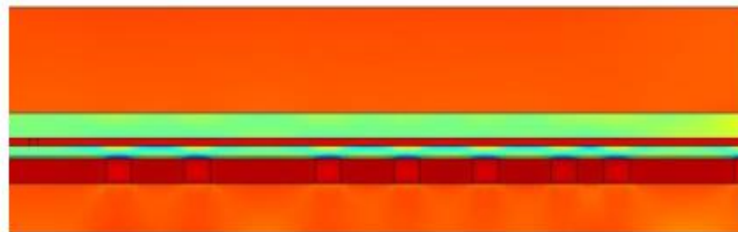
Source: Global Foundries

Global and Local Thermal Mech Stresses

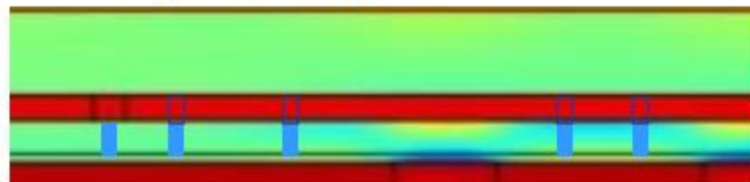




Warpage-induced stress distribution



Bump-induced stress



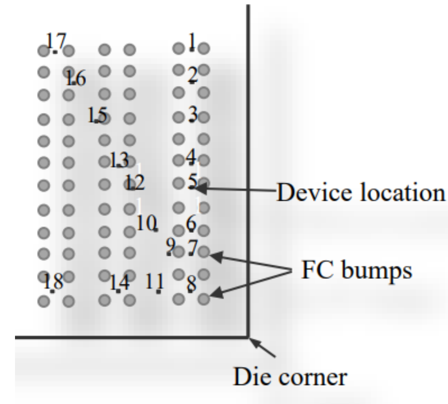
TSV-induced stress

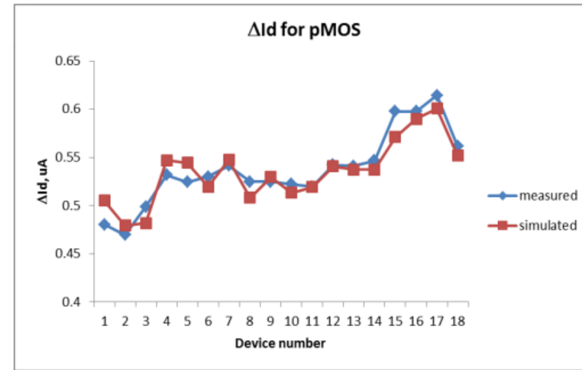
Fabrication of 3D chip stack is accompanied by generation of unintentional stresses, caused by:

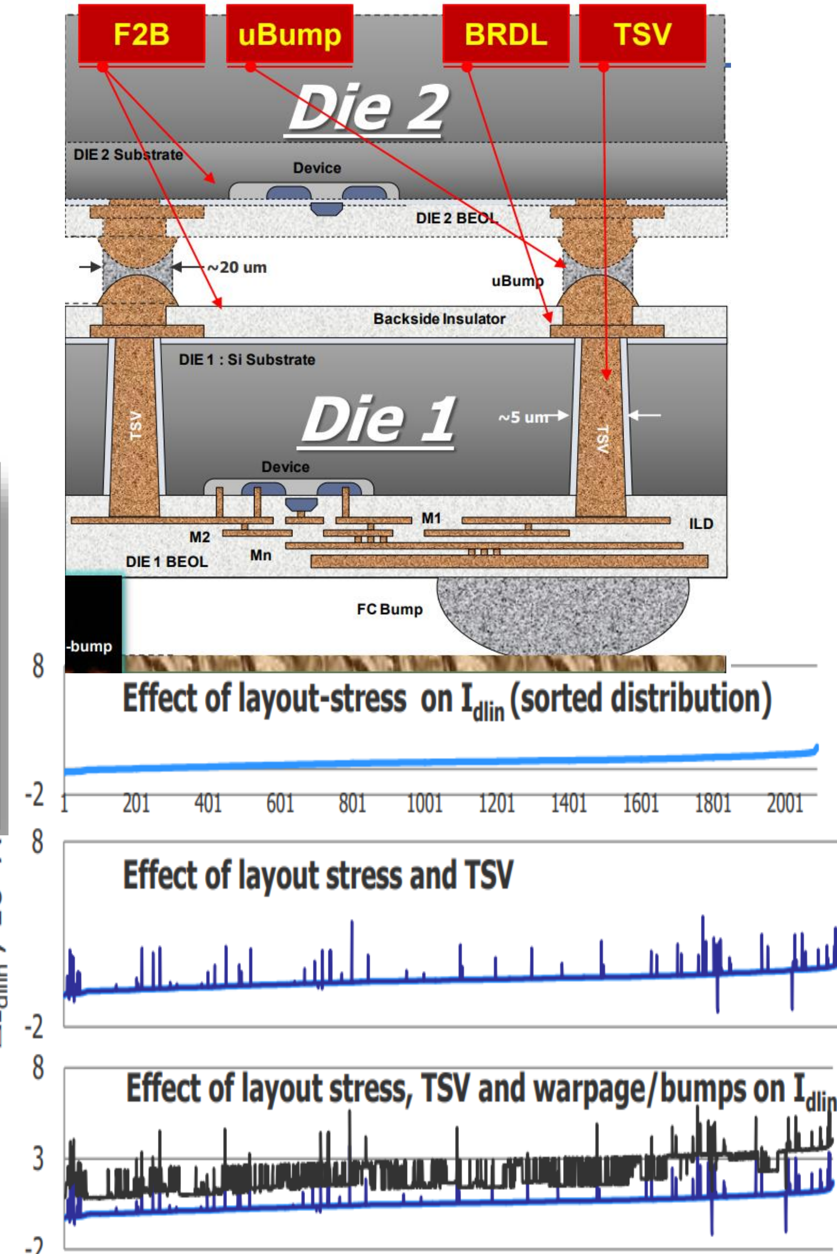
- Package warpage during the mounting – due to the mismatch of elastic properties of the layers;
- Bump effect – due to mismatch of thermo-mechanical properties of bumps and underfill;
- TSV effect – due to mismatch of thermo-mechanical properties of TSV and silicon.

Stress-Aware Modeling and Floor Planning

- Rationale for development
  - CPI mechanical stress effects on MOSFET characteristics
  - Stress generated by warpage of thin dies
  - TSV and solder bump-induced stresses
- Solutions Flows
  - Hot-spot checking
    - Supports different types of devices (e.g. digital, analog, AMS, etc.)
    - Characterized by sensitivities to stress-induced mobility variations
  - Early Floor planning analysis







Analysis and Design Flow

- Detailed analysis of stress impact on the device/circuit characteristics is performed for each hot-spot bin detected in coarse screening
- Analysis
  - Detailed analysis results: calculated mobility variation MULU0, as well as the stress components induced by TSV, CPI, and the total stress
  - Has an option to analyze the layout-induced stress effect on the device performance: Id variations caused by different layout stress sources like STI, Si(1-x),Gex, CESL, etc.
- Debug
  - Designer can determine which stress source can be responsible the out-of spec Id variations in the failed devices.
  - Move a cell containing the failed device from its original position to mitigate CPI/TSV stresses
  - Cell design modification can reduce the effect of the layout-induced stress

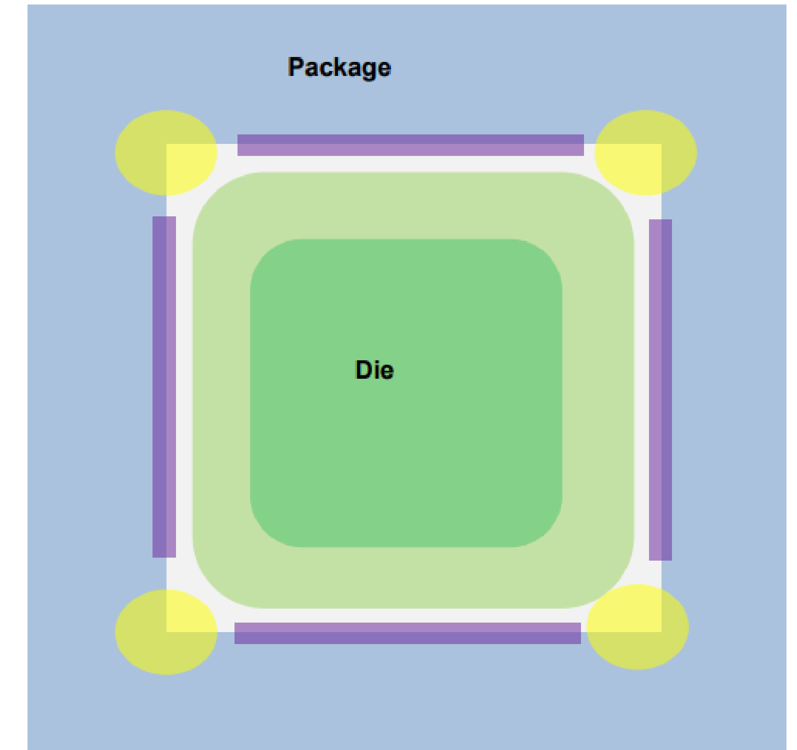
CPI Design Rule Establishment

- Design a Stress Sensitive Test Vehicle
  - Cover product needs- Different bumping schemes / via and metal densities
  - All daisy chained to detect possible failure modes
- Modeling
  - Optimize the TV design/assembly materials/process parameters
  - Understand CPI coverage
  - Understand CPI tech envelope
- Stress Tests
  - Quick TC test w/o underfill & JESD 47 standard qual tests
  - Pass/Fail – Monitoring of daisy chain resistances;
  - CSAM and X-section, etc.
- Design Rule Deliverables
  - Si node/die size/package type & size/bump material
  - Metal/via/bump density and structure
  - UBM structure and orientation
  - Substrate rigidity/CTE

CPI Test Structures

- Detect different failure modes under different stress conditions

CPI Structure	Failure Mode Detection	Chip Location
Perimeter Line	Dicing related Crack Failure	Chip Perimeter
Delamination Sensor	Corner Delamination	Corner & Center
Under Bump Crack Sensor	Delamination under bump	Corner & Center
Circuit Under Pad	Delamimation under Bondpad	Peripheral
Via Chain	BEOL Delamination	Corner & Center
Serpentines	Corrosion / Extrusions	Corner & Center
C4 Stitch/ Daisy Chain	C4-Package integrity	Corner & Peripheral
C4 EM	Electro-migration	Corner & Perimeter

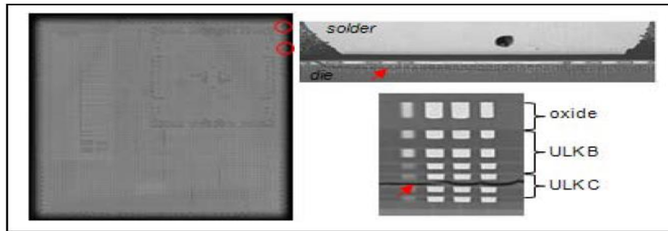


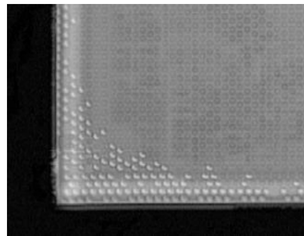
- Reliability Structures in 2.5D and 3D applications are extended by interposer / TSV reliablity chains

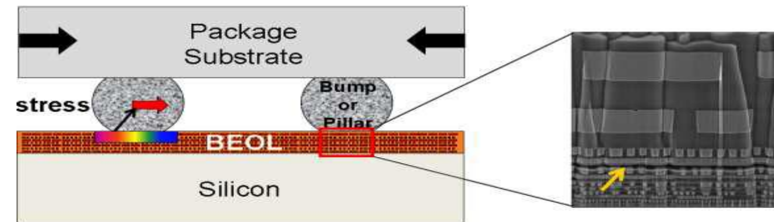
Source: JEDEC Spec

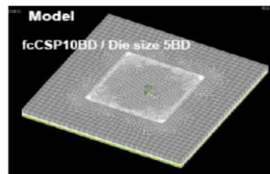
Traditional Modeling Methodology

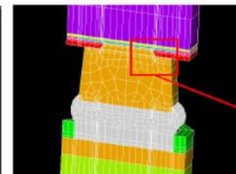
- Study on CPI Failure by Modelling

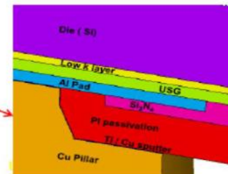


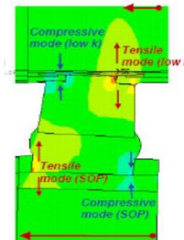


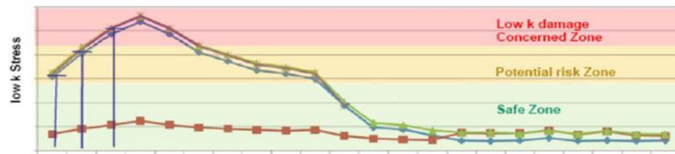


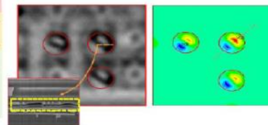










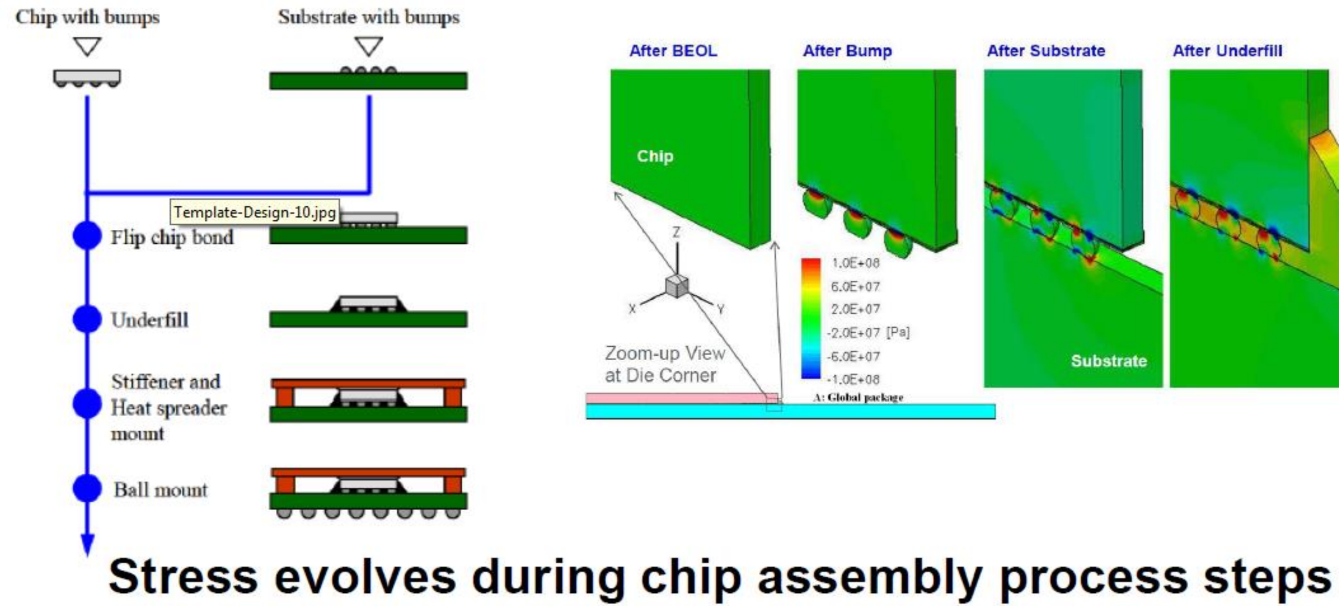


Source; Amkor

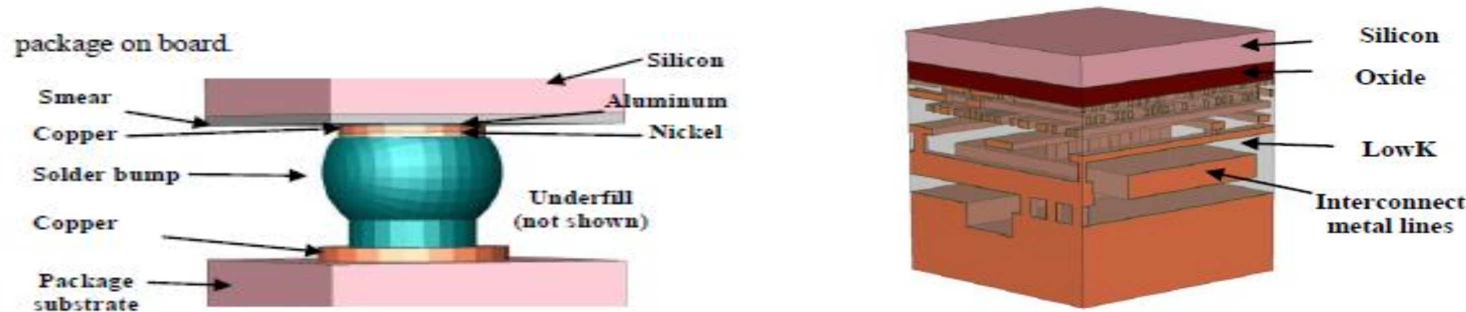
- Limitations
  - No combined assembly process + end user manufacture + field application conditions
  - No stress evolution and irreversible plastic accumulation effects
  - Not on real ASIC design
  - Not on interconnect level
  - CPI failure is pad structure dependent

Multilevel Simulation Model Details

- Flip chip assembly process and stress evolution



Stress evolves during chip assembly process steps

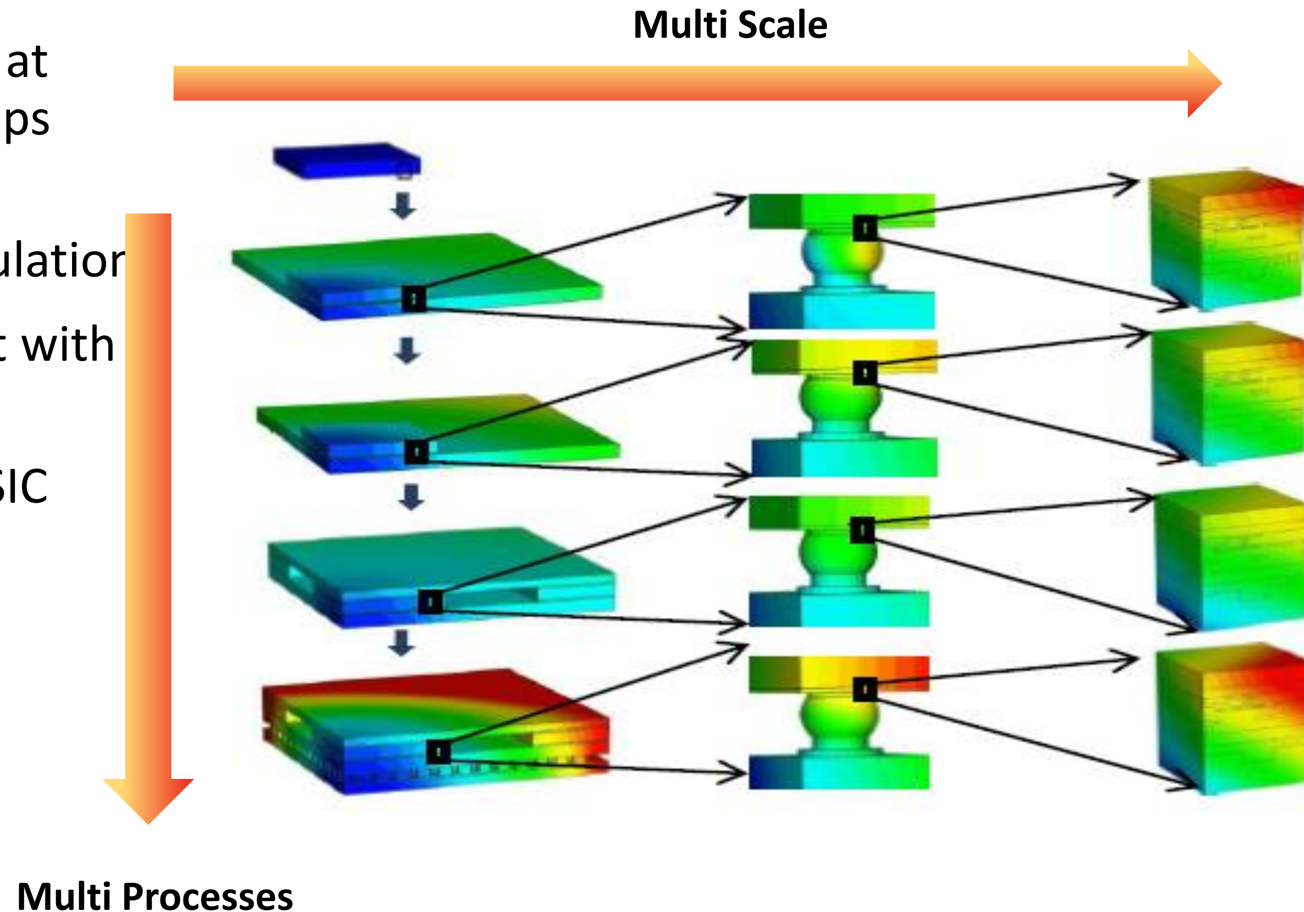


Crack at interfaces of Oxide/Low k/ELK

Source: Richard Rao, Marvell

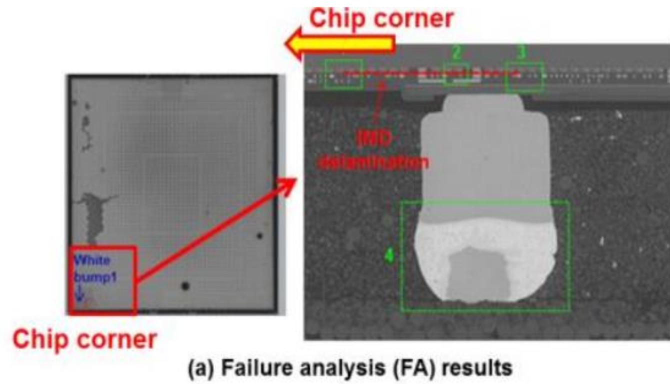
More Comprehensive Simulation Methodology

- Multilevel modeling at different process steps
- Irreversible plastic deformation accumulation
- Cracking assessment with energy release rate
- Import the actual ASIC GDS layout file

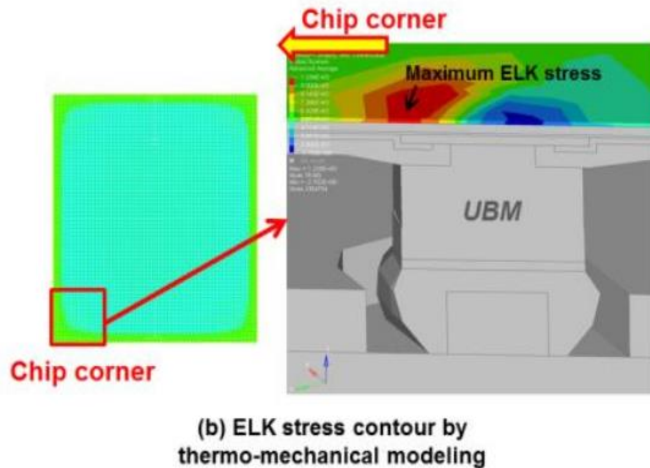


Source: Richard Rao, Marvell

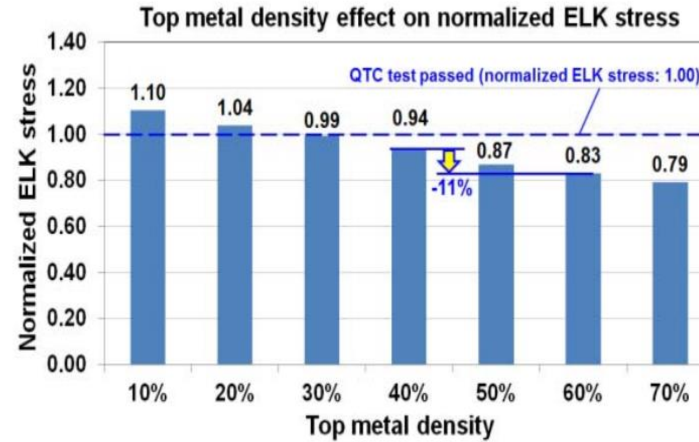
Effect of Metal Density and Bump Density on ELK Stress

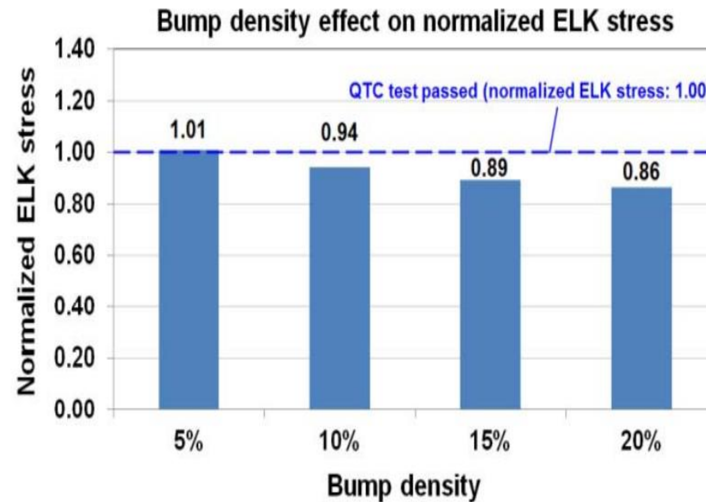


(a) Failure analysis (FA) results

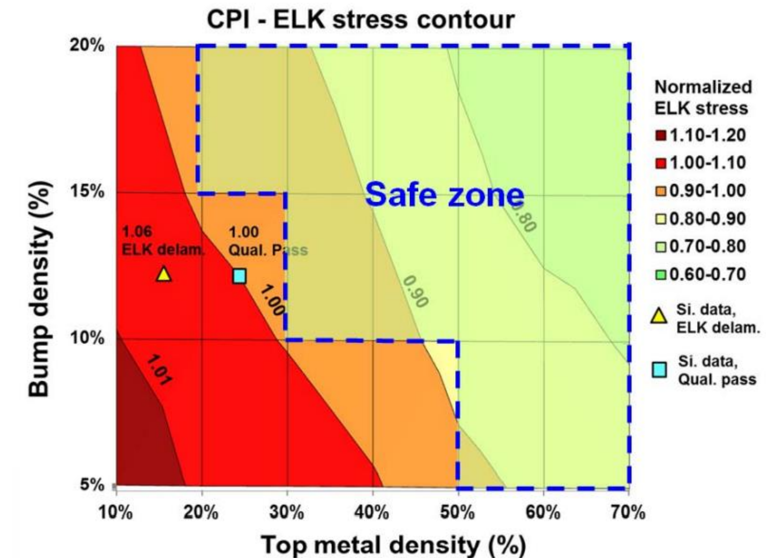


(b) ELK stress contour by thermo-mechanical modeling



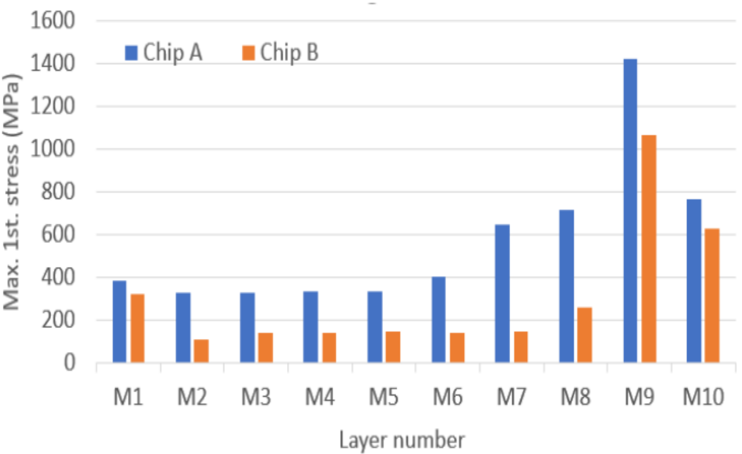


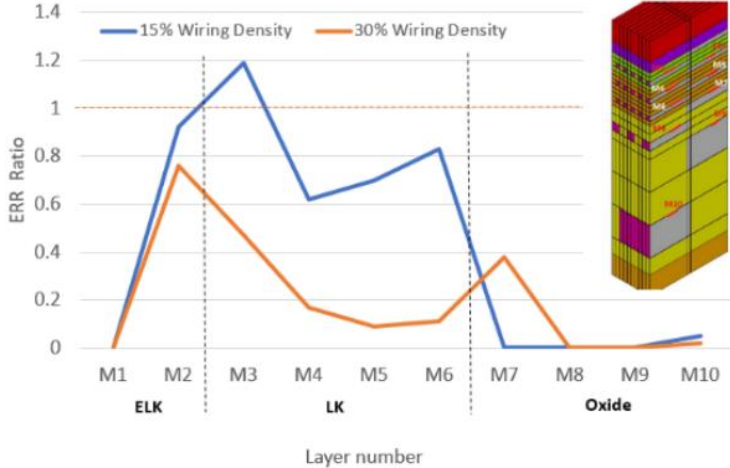
Bump density (%)	10.7	10.1
Top metal density (%)	25	15
QTC test data	Passed	ELK delamination
Normalized ELK modeling stress	1.00	1.06



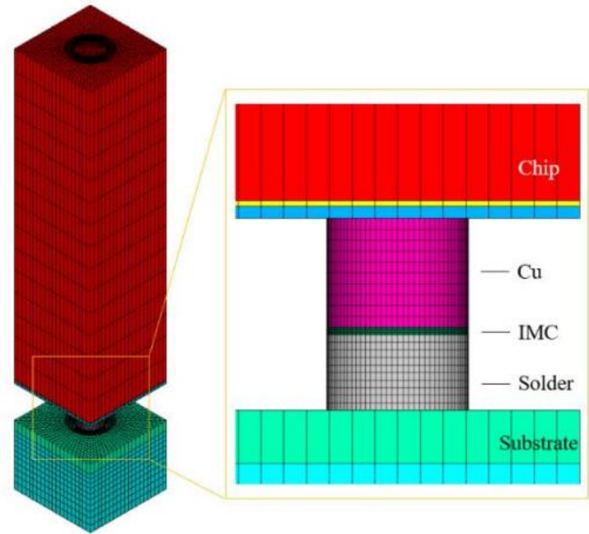
Source: TSMC and IME Singapore

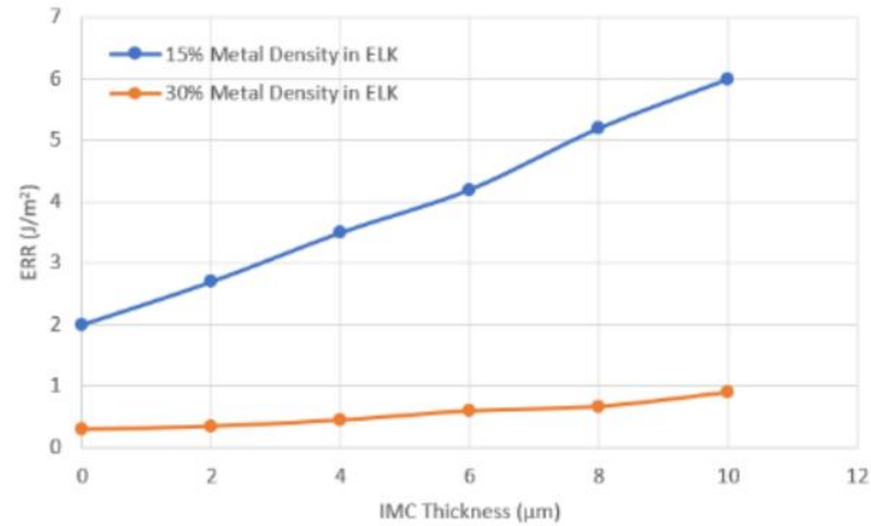
CPI Stress vs Metal Density and IMC Thickness





ERR Ratio = ERR/Critical ERR
Critical ERR is dependent on the layer interface

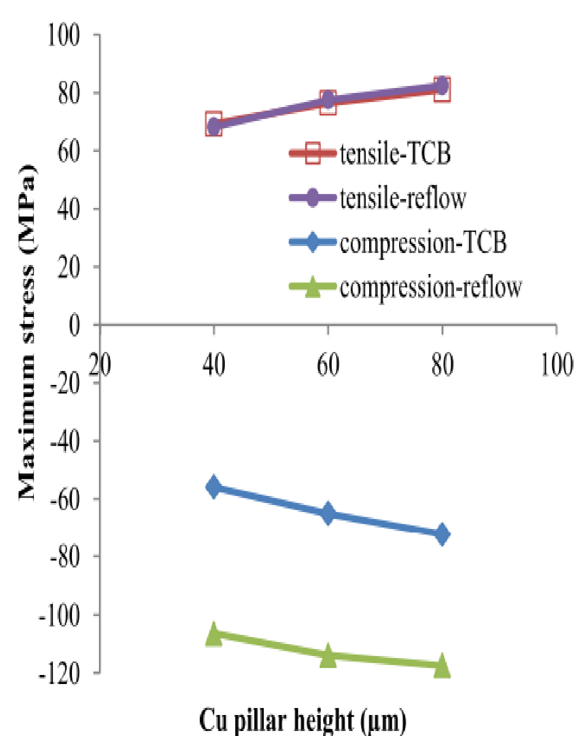


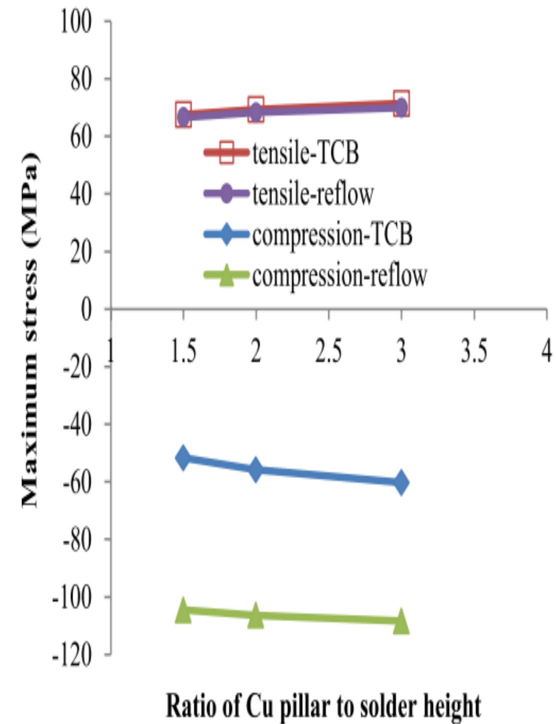


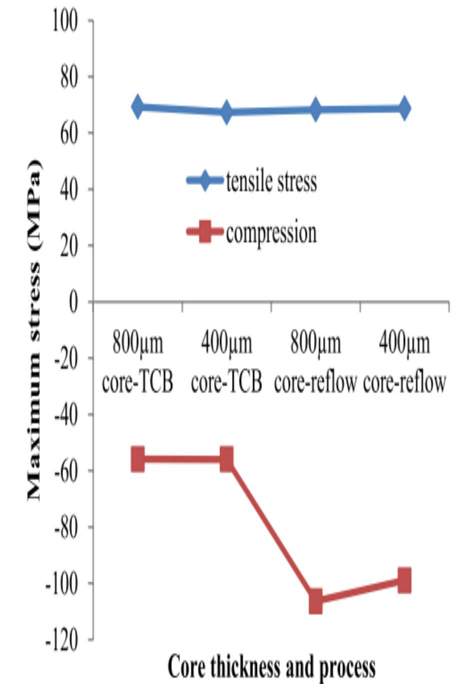
Marvell and UT Austin

Effect of Cu Pillar and Solder Height on ELK Stress

Shorter Cu pillar and smaller ratio of Cu pillar to solder height result in lower low-k stress

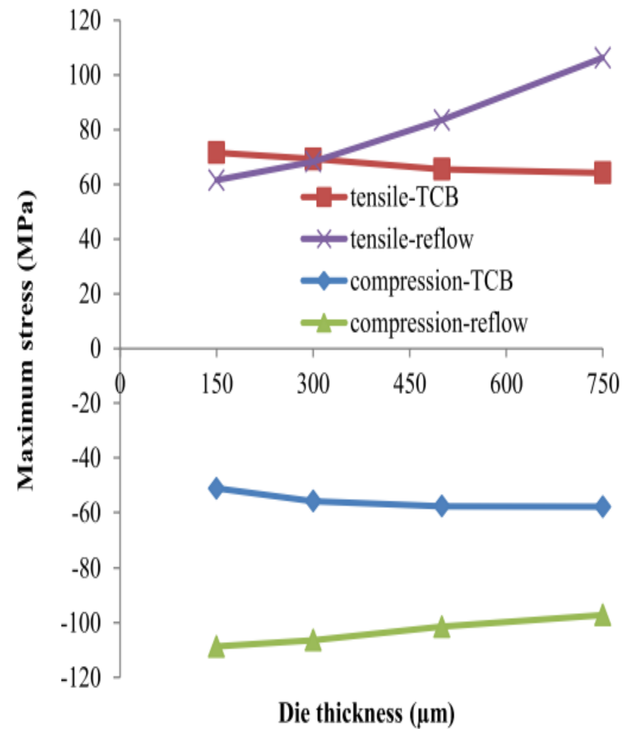


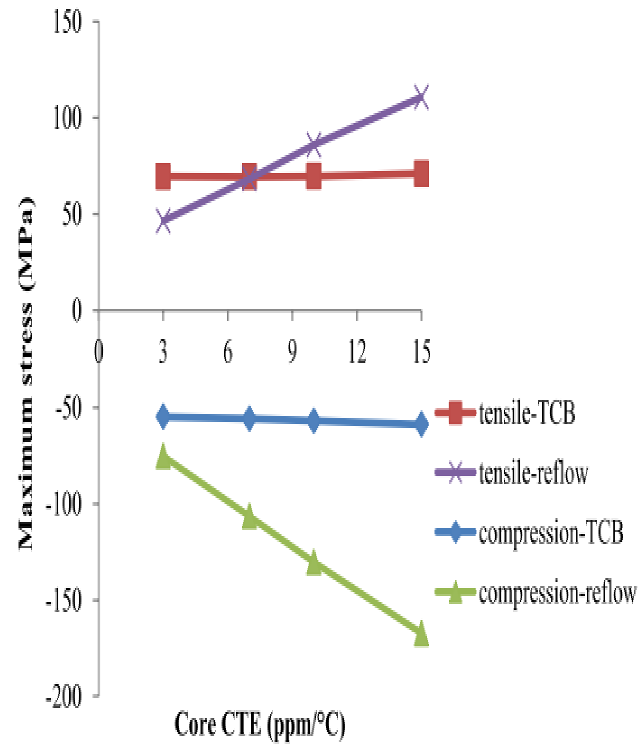


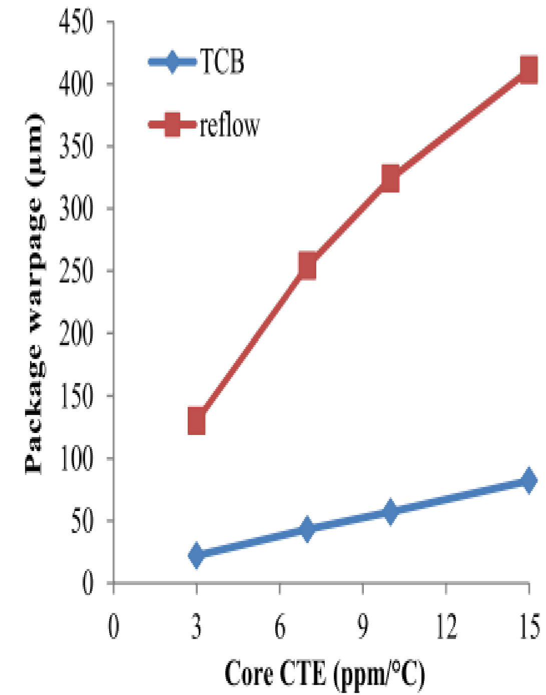


Source: Marvell and UT Austin

Effect of Die Thickness and Substrate Core on ELK Stress







CPI Sensitivity Verification Deliverables

- Bump and Metal Design Rules
  - Each Si node
  - Die size and thickness
  - Min bump pitch/size
  - Bump global and local density
  - Bump orientation (oblong Cu bump)
  - UBM structure and dimension
  - UBM/Substrate SRO ratio
  - Passivation opening
  - Top metal density/gap structure and metal density gradient
  - Local and global metal and via density
  - With or Without PI
  - Package type requirements BGA, WLCSP or WLP, etc.
  - Substrate core thickness and CTE
  - Metal Density and Density Gradient
- CPI risks are mainly on the Si, bump, substrate and package designs
  - Difficult to fix by assembly process only

CPI Test Vehicle Execution

- Test Vehicle Design
  - Major failure modes and appropriate structures to detect failures
  - Major variables to consider
  - CPI corner definition
  - CPI coverage
- Phase I
  - Design big DOE matrix to include all major variables
  - Use CPI simulations to narrow down the corners
  - QTC and mini qual to find out the best corners
- Phase II
  - Verification of best corners
  - Extract design rules
- Phase III
  - Final qual
  - Reliability failure probability analysis

CPI Stress Factors

- Fab Process Induced Residual Stresses
- Assembly Induced Stresses
- Static Thermal Loading
  - Heating by power consumption in high performance devices
- Cyclic Thermal Loading
  - Environmental temperature cycling
- Heating by local power switch on/off
- Humidity Loading
  - In general packages are not hermetic, soaking by moisture has to be considered, Silicon chip has to be hermetically sealed
- Sequence of Several Load Steps

Gaps between CPI Test Vehicle and Real IC Circuits

- Test structures don’t represent the actual circuits
  - Uniform metal density
  - Metal topology
- Can’t cover the process variations
  - Earlier failure probability
- Cover the environmental stress conditions
  - Localized self heating temp induced CPI failures

ERR vs Metal Topology

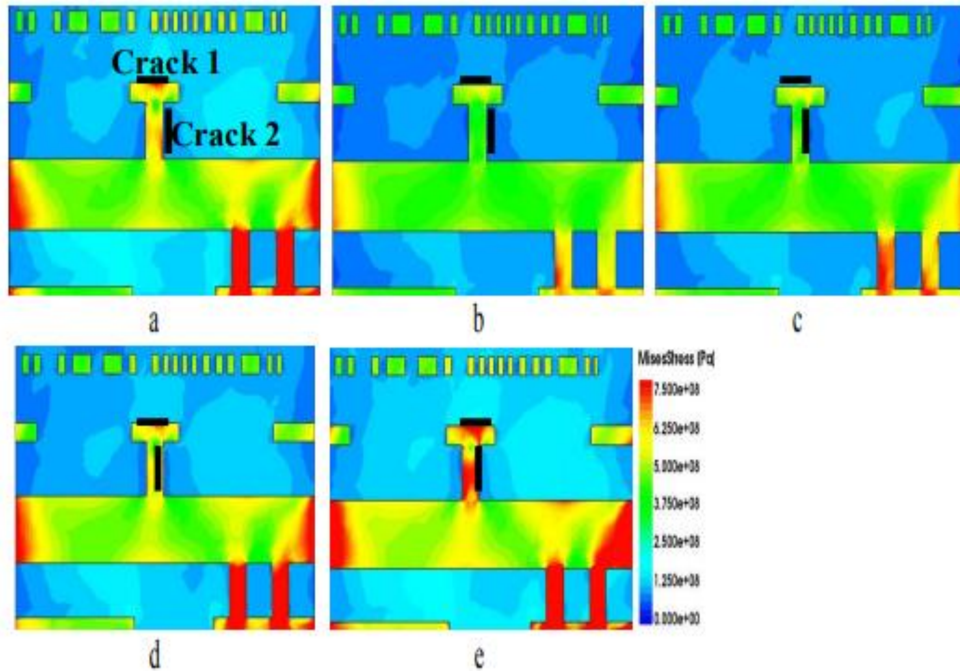


Figure 10. Interconnect Driving Force Evolution. a. Flip chip attachment; b. Underfill; c. Lid Attachment; d. First Surface Mount; e. Two additional IR reflows.

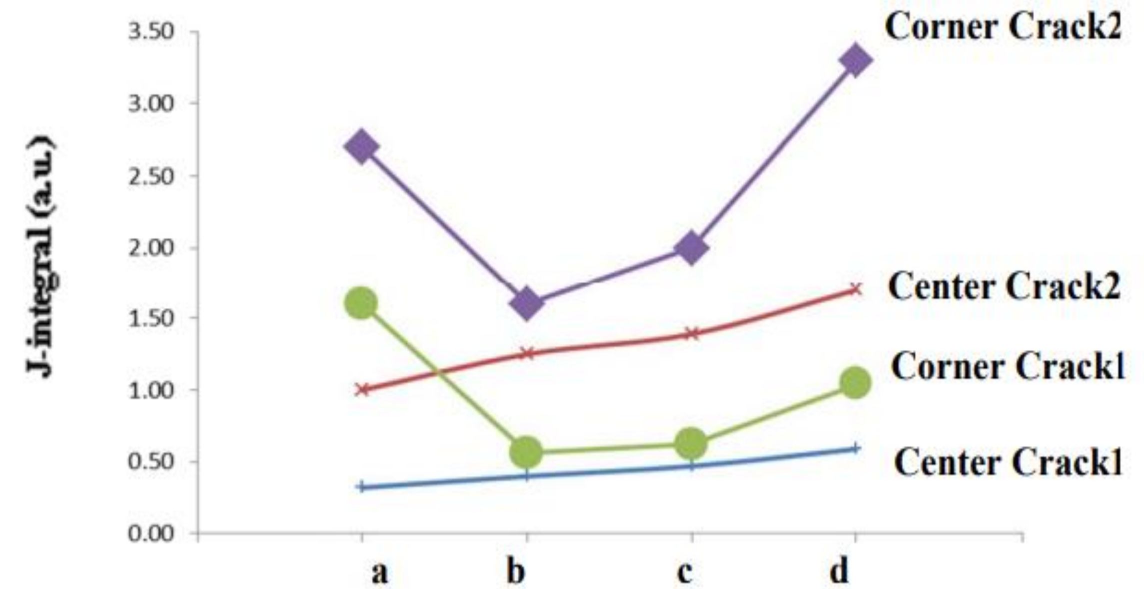
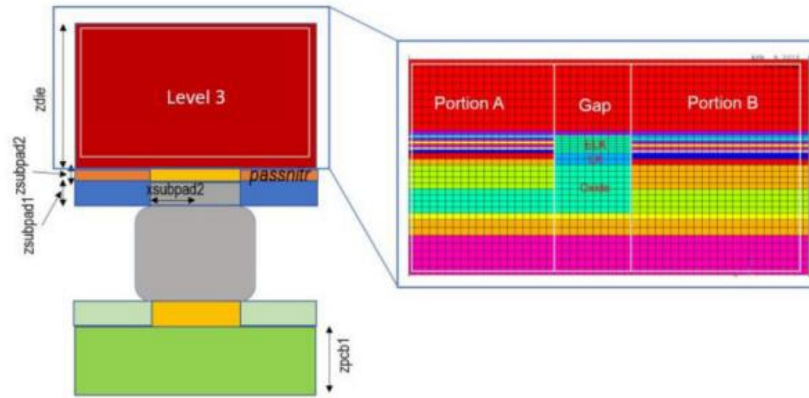
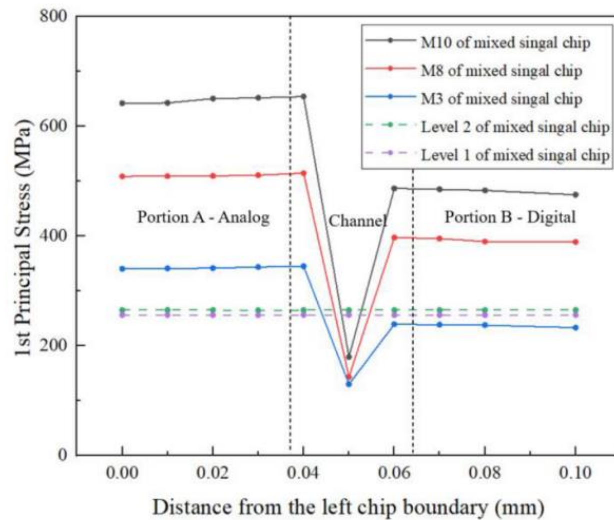


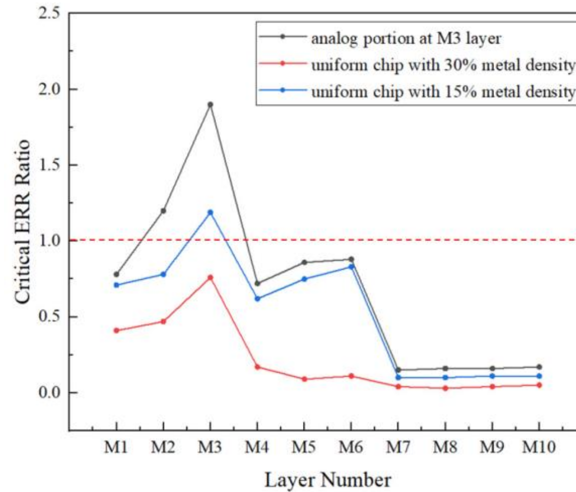
Figure 11. Energy release rates (J-integral) for pre-assumed cracks at different assembly steps. a. Bump attachment; b. Underfiling; c. Lid attachment; d. Surface Mount on PCB.

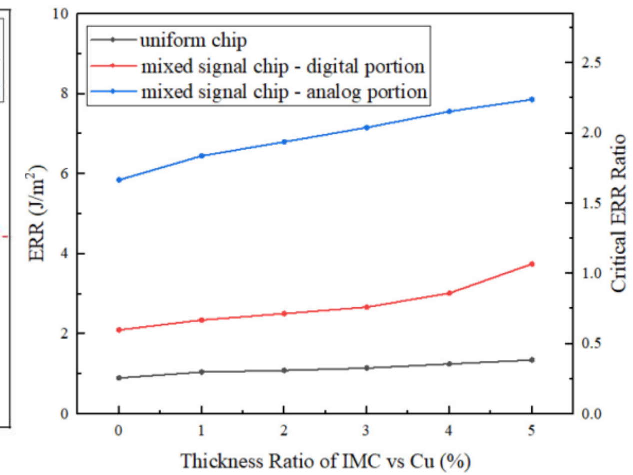
Metal Density Gradient Effect on ELK Stress



Layer Number	Materials	Metal Density Portion A	Metal Density Channel	Metal Density Portion B
M1-M3	ELK, Cu	15%	2%	20%
M4-M8	LK, Cu	25%	2%	30%
M9-M10	Oxide, Cu	45%	2%	50%







ERR Ratio increases from 1.2 to 1.9 at analog to channel transition

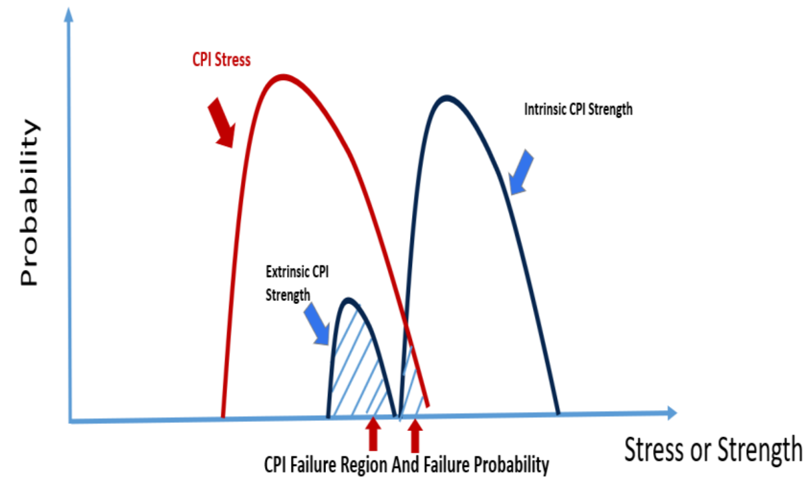
Source: Marvell and UT Austin

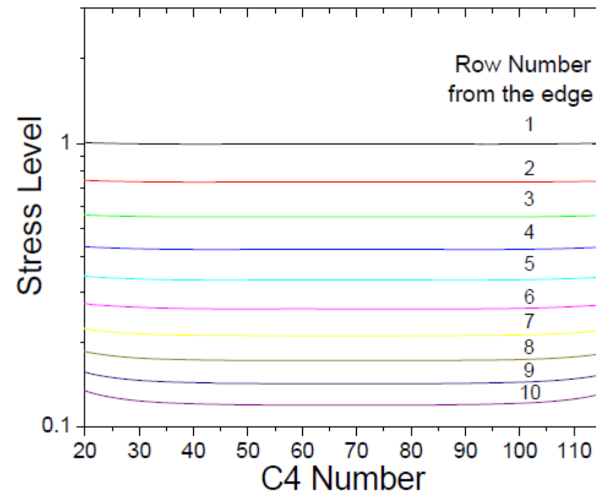
Product CPI Qualifications

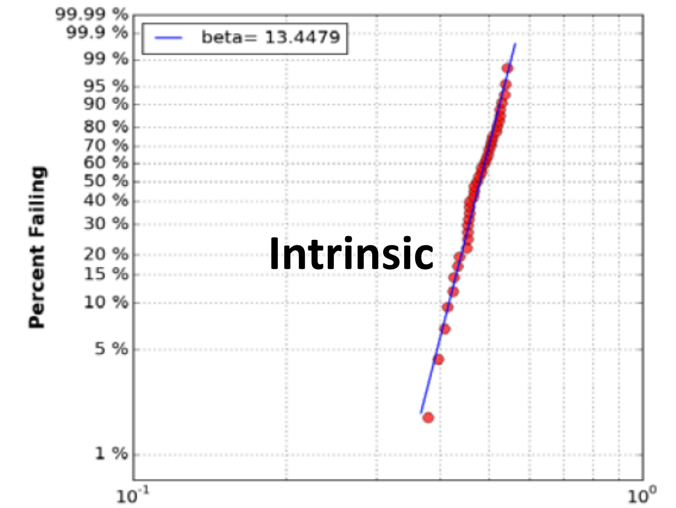
- Product Qual after the CPI Technology Qual
- Assembly Qualifications
  - Die shear/Die pull
  - CSAM
- Quick TC Test /Hammer Test
  - TC test w/o underfilled part
  - 30 ~50 cycles of -45C/60C
  - To reveal potential CPI failures
- JESD47 Stress Tests on Component Level
  - Precon/Temp Cycling/UHAST/HTSL
  - Powered TC test for high power devices
  - Power cycling for devices w/ frequent power on/off

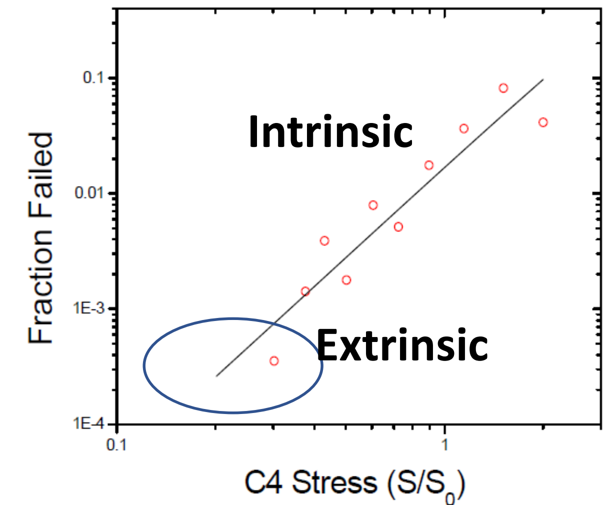
CPI Induced Failure Rate Projection

- Construct the stress distribution plot
- Construct the intrinsic and extrinsic strength plot









CPI Challenges on Advanced HI Packages

- Big FCBGA
- High speed pins even on small die
- 2.5D with Si Interposer
  - Multiple assembly process induces accumulated stress
  - ILD cracking in interposer, molded vs non molded
- 2.5D with RDL Interposer
  - Multiple assembly process induces accumulated CPI stress
- Silicon Photonics
  - Die attach process – Moisture expansion induced stress; stress affect the optical refractive index.
  - C4 bump and TSV induced stress concentration

Summary

- CPI is becoming a critical reliability issue due to adoption of advanced Si node and new packaging materials
- Many factors affect CPI failures, stresses and under bump metal structures are the key factors
- From IC product prospective, the conventional FEA approach is not adequate to address this reliability issue because it can’t simulate the real under bump structure
- TSV/u-bump integration added additional CPI failures
- TSV induced need to be well analyzed and managed to minimize the e-CPI effect
- Need bring circuit designers, foundry and OSAT together to co-design the CPI reliability

Si Photonics Products Reliability Challenges

- SiP (Silicon Photonics) products are new to market – need to understand and scope out scalability, manufacturability, and long-term reliability
- Hybrid SiP lasers reliability demonstration and monolithic integration for better integrateability and performance
- Challenges arise due to high level of integration to meet product, process, and customer use condition requirements

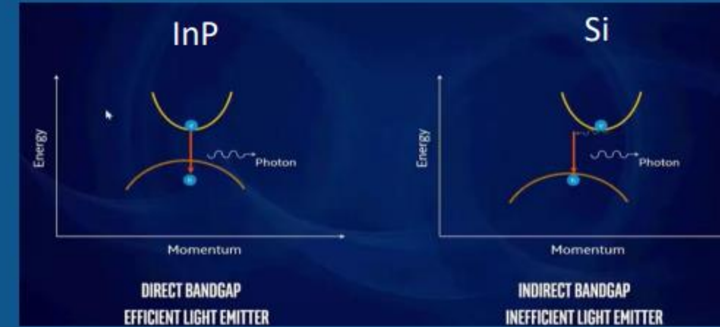
What is Silicon Photonics?

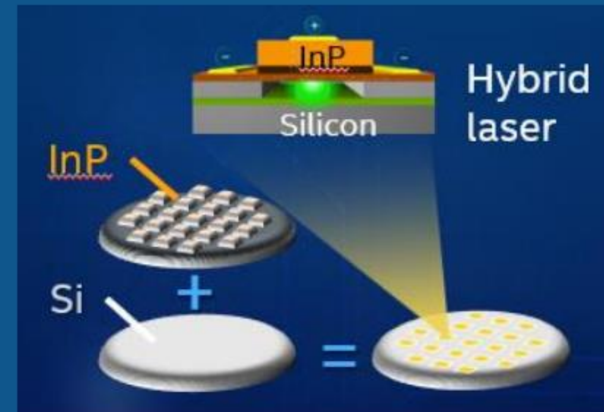
What is Silicon Photonics?

Silicon Photonics = *Photonic solutions using silicon as the optical medium*.

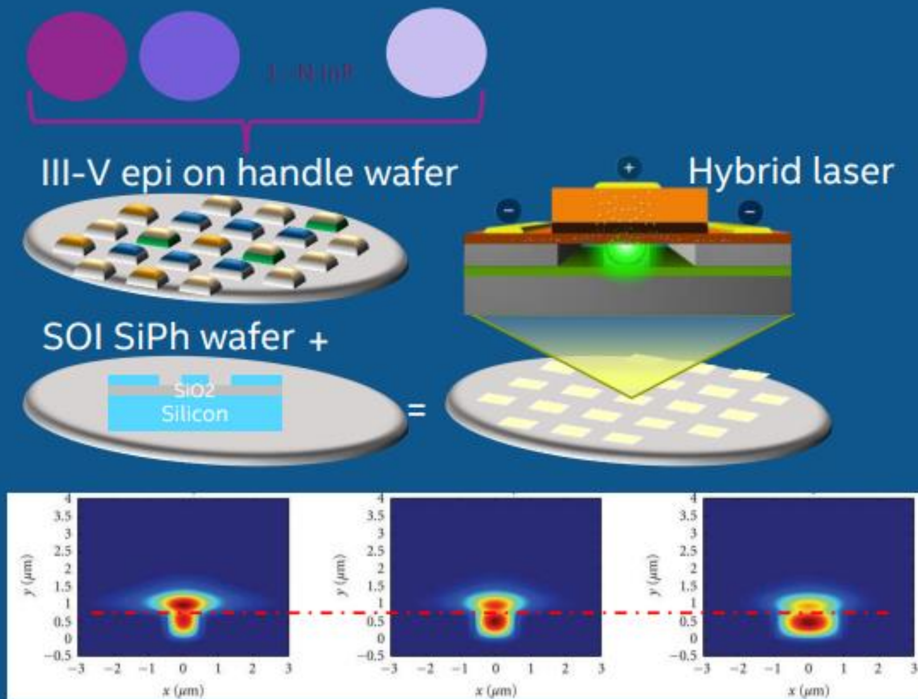
- Silicon is inefficient in emitting light
  - Energy band diagram, for Si minimum of CB and max of VB don't line up
  - Not easy for electrons to fall into VB
  - Makes Si indirect band gap material
- InP (III-V) is direct band gap material

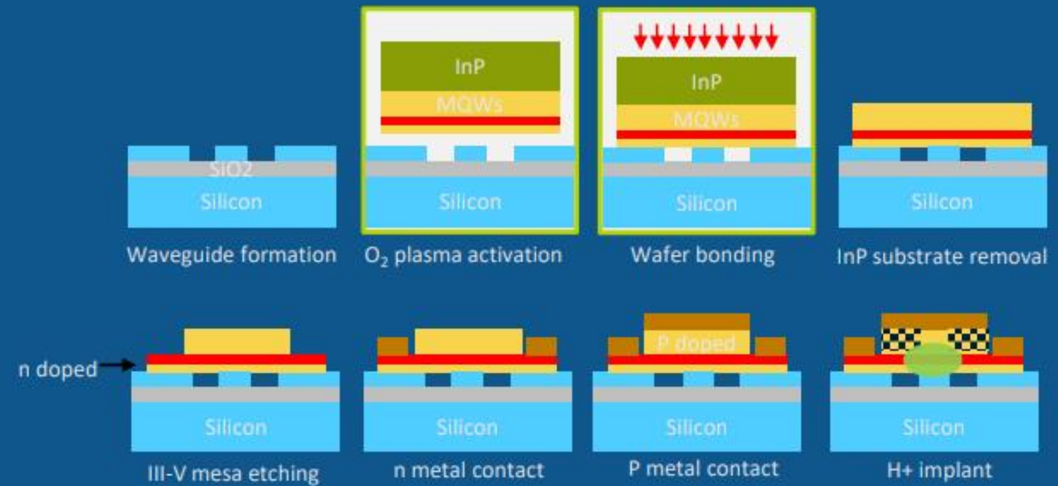
Intel's approach: *InP – Si Hybrid*





Heterogeneously integrated lasers (Hybrid Laser)





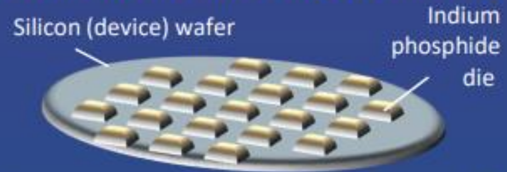
P. Doussiere et al. (Intel SPPD), GFP 2017

- 300 mm wafer bonding
- Tight CMOS process control
- Lasers photolithographically aligned to Silicon Photonic circuits; evanescent coupling <0.5 dB loss
- Low optical propagation loss due to reduced overlap with p-doped material (< 5 cm-1)
- Design of IIIV epi can be optimized on different regions PIC and / or wafer => WDM lasers, SOAs, etc.

Presented: OFC 2023 - Advancements in heterogeneously integrated silicon photonics for IMDD and coherent data transmission

Delivering Optics At Silicon Scale

LASER FABRICATION

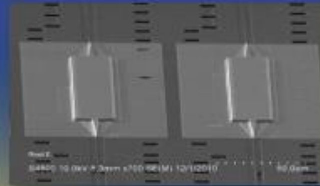


Plasma activation and bonding: InP die are bonded & transferred in parallel to device wafer

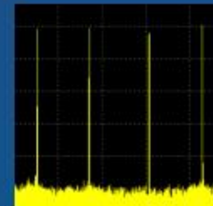
InP substrate removal: only active epi layers remain on device wafer

InP for lasers, SOAs, PDs

SILICON INTEGRATION

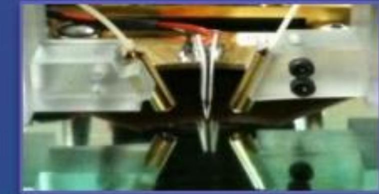


- Advanced CMOS manufacturing at Intel fabs on 300mm wafers
- Capable of multiple optical wavelengths and integration of multiple optical components



SILICON SCALE

Optical



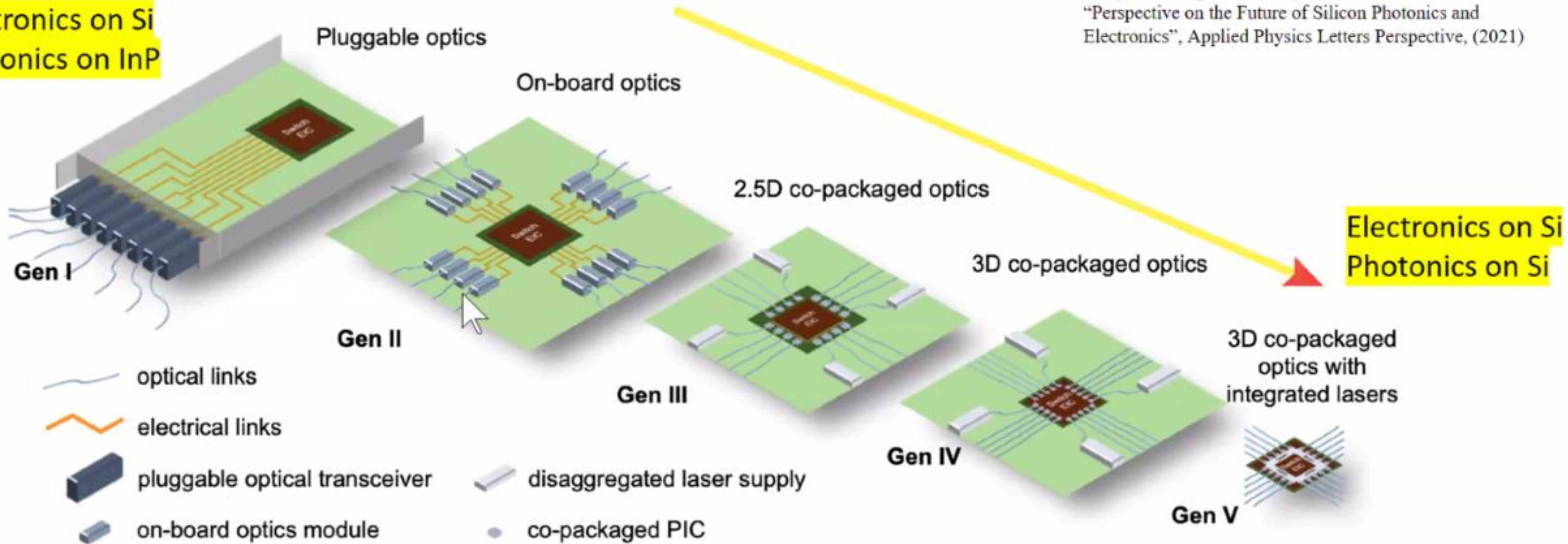
Electrical

RF

- Automated on-wafer optical, electrical, and high-speed test
  - Wafer level burn-in

Robert Blum, "The Promise of Co-Packaged Optics: Paving the Way for Improved Power, Size, and Cost," IEE/UCSB Energy Efficient Cloud and Data Center Workshop, 2020

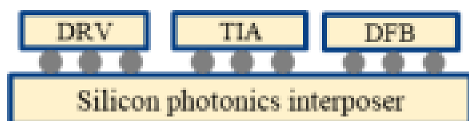
Merging Photonics and Electronics



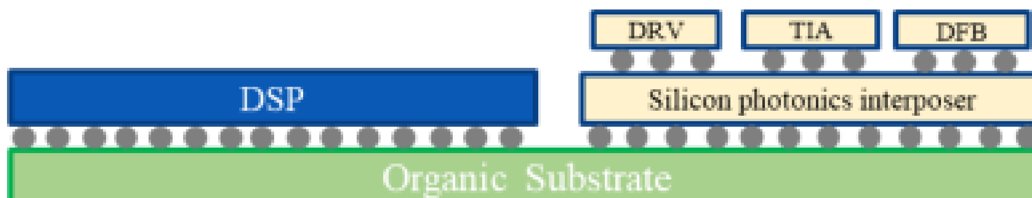
Generations of optics and the evolution of co-packaging technologies used in data center applications. The generational progression drives tighter integration between network switching and optical I/O that will probably culminate with 3D co-packaged optics with integrated lasers on chip.

Heterogeneous Integration of Silicon Photonics Package

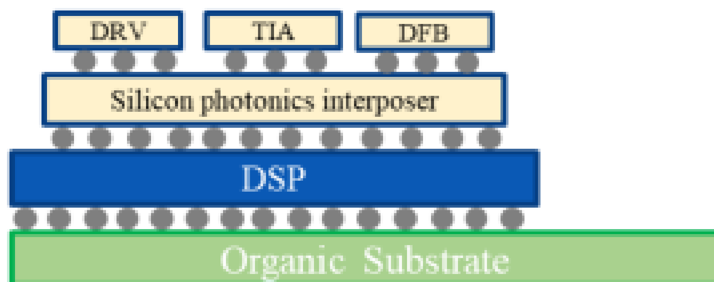
2D
Integration

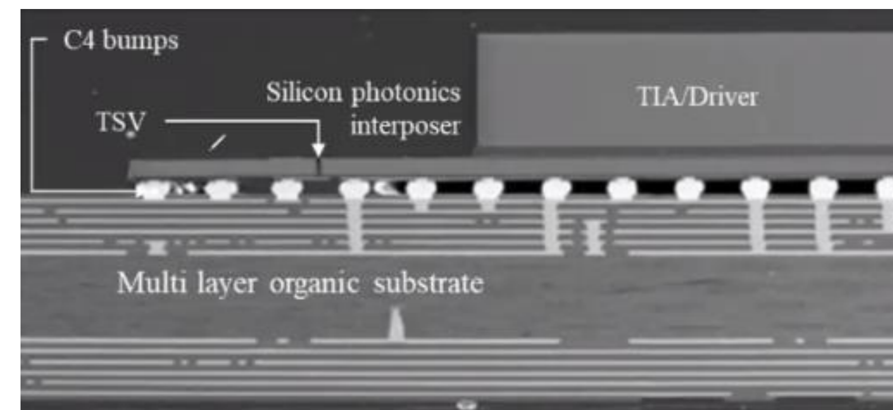


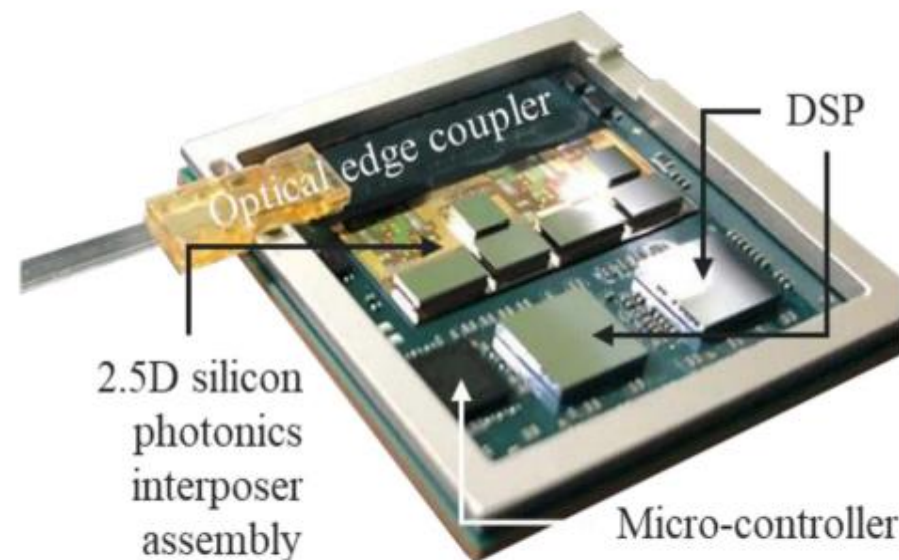
2.5D
Integration



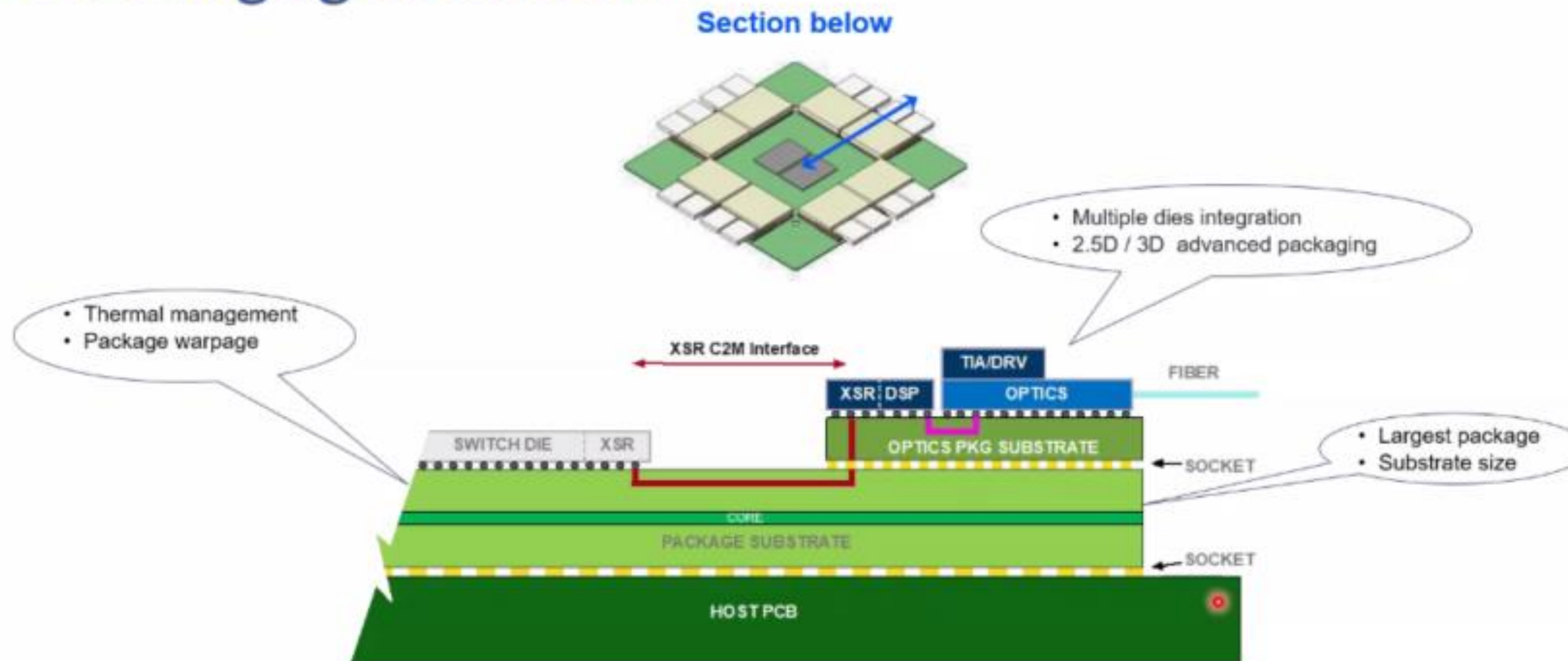
3D
Integration





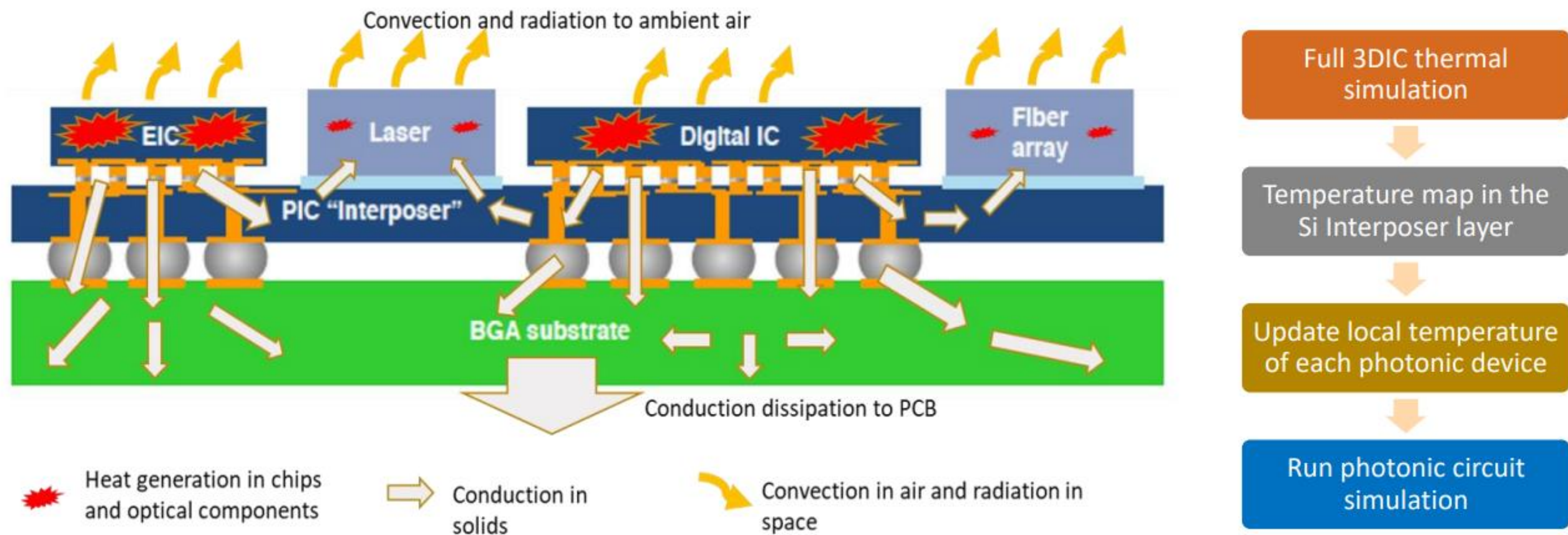


Co-Packaged Optics



Source: Meta

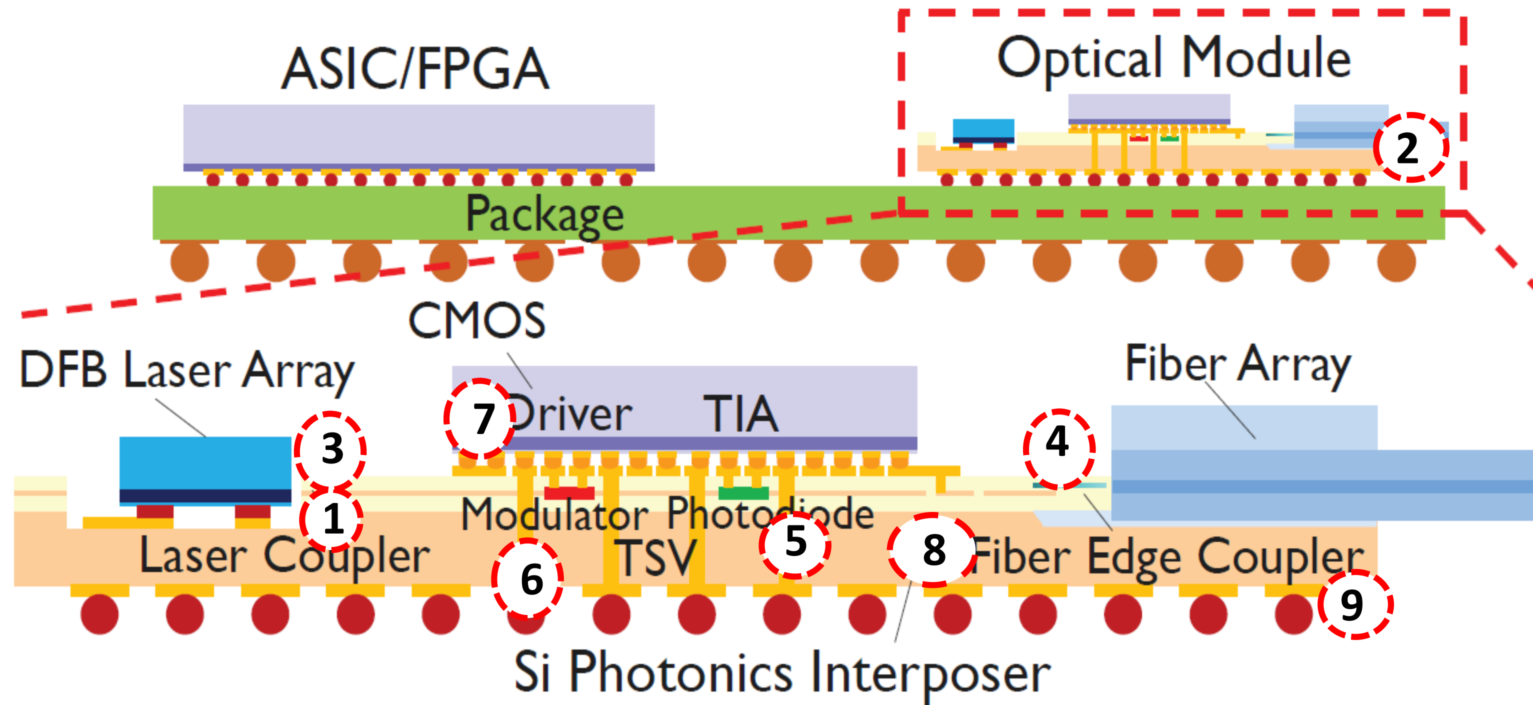
Thermal Simulation of 3D Silicon Photonics Package



"Electronic-Photonic IC Co-Design with Signal/Power Integrity and Thermal Simulation for Silicon Photonic 3D IC", J. Youn, J. Pond, N. Chang, et al., best paper candidate, DesignCon 2021.
"Optical and Thermal Simulations for Integrated III-V/Si Heterogeneous Lasers of Silicon Photonics System", S. Cheung, D. Liang, J. Pond, N. Chang, et al., DesignTrack, DAC, 2021.
"Thermal Tuning Power Budgeting With Statistical and Temperature Variation for Microring-Based DWDM 3D Silicon Photonics", J. Youn, J. Pond, N. Chang, et al., DesignTrack, DAC 2022.

SiPho CoWoS Potential Reliability Failure Modes

- **1.** SiPho interposer cracking
  - Laser trench corner stress concentration FIB cut
- **2.** UF1 Underfill cracking and delamination
- **3.** LD to SiPho Coupling degradation
- LD attachment degradation
- **4.** Fiber array to SiPho Coupling Degradation
- **5.** TSV and TSV/DSV interface cracking
- **6.** TSV/RDL to C4 bump interconnect open
- **7.** uBump cracking
- **8.** Local Stress effect on optical device performance
  - Less sensitive for large devices
- **9.** PI Passivation(15um) for C4 bumping – pop corn
- **10**. UF2 Underfill cracking and delamination
- **11.** Warpage Induced Failures
- **12**.Residual stress within Sipho die
- **13.** PLC delamination
- **14.** MPD/Heater performance degradation



Silicon Photonics Package Qualification

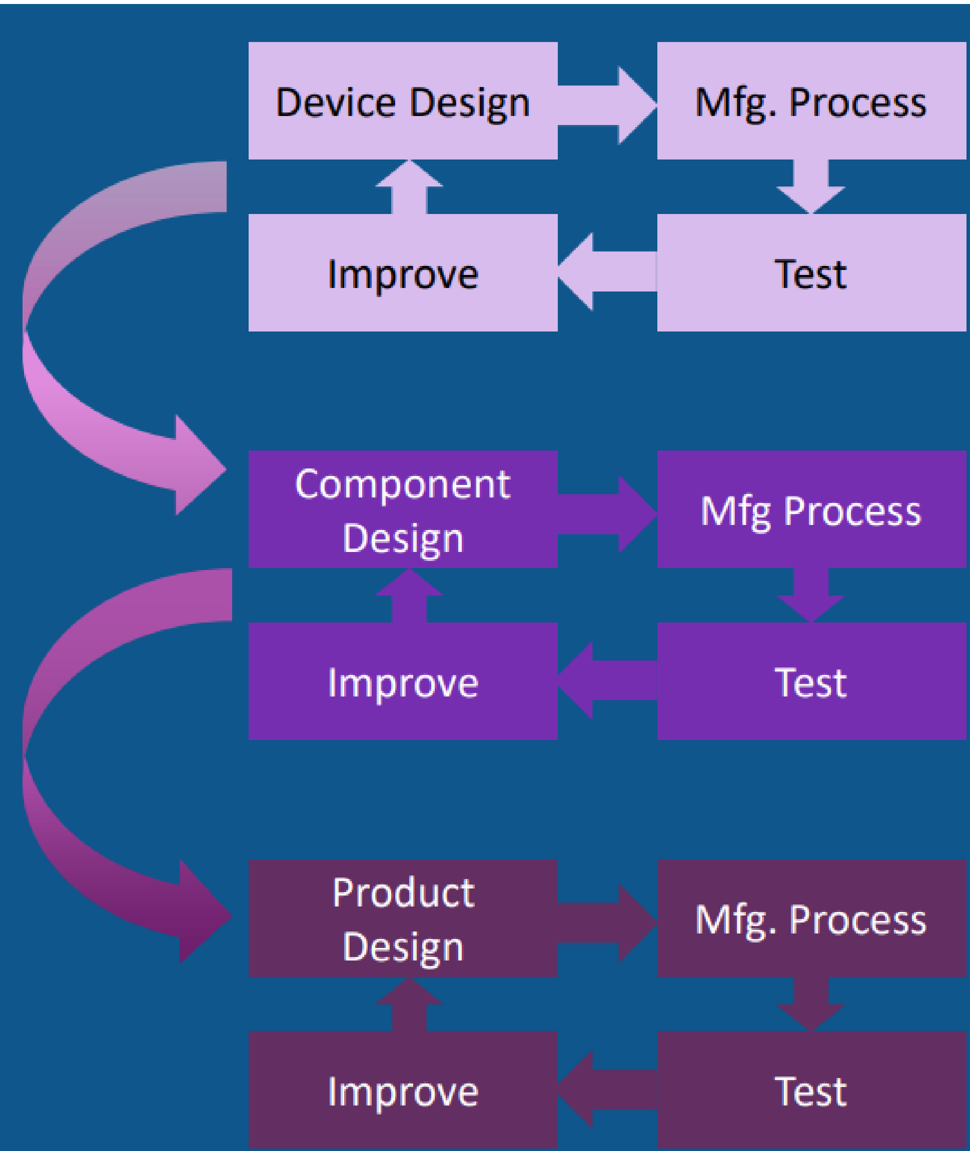
- Laser diode HTOL
  - Long term accelerated life test
- Through Silicon Via (TSV) qual
  - Electromigration
  - Thermal mechanical reliability
- SiPho chip derisking and qual
  - ESD test
  - HTOL Life test
- Laser Diode on SiPho derisking and qual
  - Laser diode integrated on SiPho die
  - HTOL test on LD Integrated on Sipho
- SiPho mounted on organic substrate qual
  - Thermal mech integrity
- Fiber assembly alignment qual
  - Thermal and mechanical integrity qual of fiber alignment to SiPho
- Integrated module qual
  - Thermal mechanical and mechanical
  - Electrical and optical

Muti-Level Reliability Qualification Paradigm

1) Device level intrinsic reliability characterization
   a. Biased devices: Laser, Photodetector, Phase shift diodes, Heaters, MIM capacitors,…
   b. Unbiased devices: WGs, couplers, etc.
   c. Knowledge-base + standard-base stresses

2) PIC level
   a. Full channel integrated effects
   b. Defect reliability/early life assessments
   c. Environmental stresses
   d. Knowledge-base + standard-base stresses

3) Module level
   a. Fully integrated effects
   b. Interoperability
   c. Knowledge-base + standard-base stresses



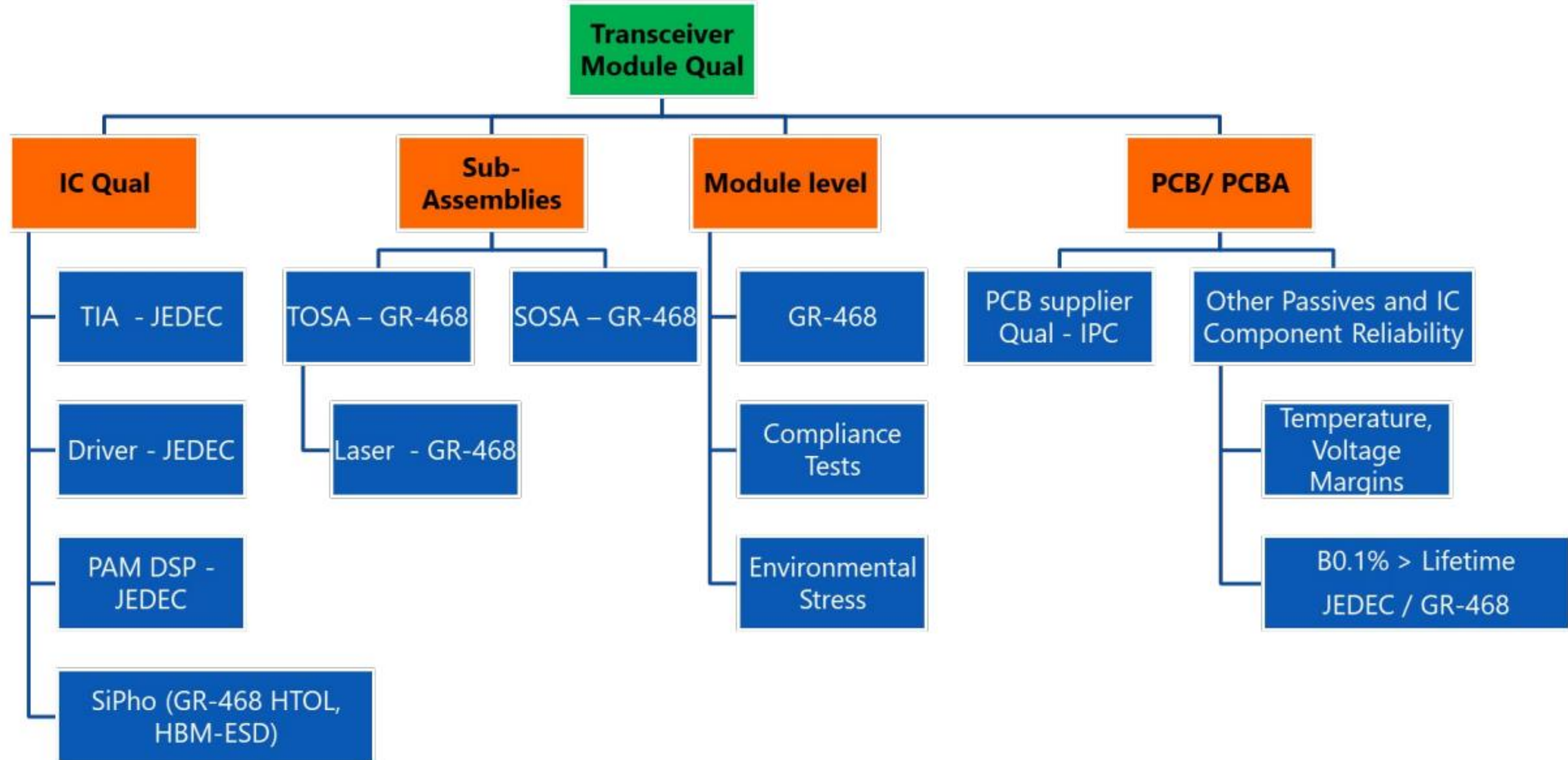
Relevant Reliability standards

- Telcordia GR-468-CORE: Optoelectronic Reliability
- Telcordia GR-357-CORE: Generic Component Reliability
- Telcordia GR-1221-CORE: Passive Optical Component Reliability
- Telcordia SR-332: Reliability Prediction
- JESD47: Stress-Test-Driven Qualification of Integrated Circuits
- MIL-STD-883: Test Method Standard Microcircuits

Other standards/testing procedures are also applied per customer requirement(s)

- AEC Q102: Failure Mechanism Based Stress Test Qualification for Discrete Optoelectronic Semiconductors in Automotive Applications
- IATF 16949: Automotive Quality Systems Management
- ISO 26262: Functional Safety
- Internal and Customer requirements

Multi-level SiPho Module Qualification Tests



Component Reliability Requirements

PIC Component & Laser qualification focuses on Telcordia GR-468

- Requirements are low volume, long duration stresses
- Not sufficient to determine actual reliability goals, e.g. 100 FIT
- Additional reliability stresses or sampling often required based on failure modes, use conditions and FMEA findings
- Validate with customer RMA data

component	Stress Type	Condition	Duration	GR-468 min ss
Tx/Rx	HTOL	max op T, max op bias or power (70C min for OC, 85C min for UNC)	2khr required, extended to 5khr for info	22
	THB	85C, 85%RH, nominal bias	1khr required, extended to 2khr for info	11
	TC	Tmin/Tmax storage temp, no bias	100 cyc, 500 cyc for info	11
	HTS	Tstorage,max, no bias	2khr	11
	LTS	Tstorage,min, no bias	72hr	11
	THuB	85C, 85%RH, no bias	500h required	11
	BCMR	-10/65C, 95%RH for T>25C, nominal bias	20 cycle required only for uncontrolled environment use (as opposed to central office environment)	11
	ESD	HBM	find tolerance limit	6
Photodiode	HTOL	175C, 2x Vop or 75% Vbr	2khr	22
	THB	85C/85%RH, Vop	2khr required for non-hermetic use	11
	TC	Tmin/Tmax storage temp, no bias	100/300cyc required, 500cyc for info	11
	THuB	85C/85%RH, unbiased	2khr required for non-hermetic use	11
Laser	HTOL	max op T, max op bias or power (70C min for OC, 85C min for UNC)	2khr required, extended to 5khr required	22
	THB	85C/85%RH, 1.2x Ith	2khr required for non-hermetic use	11
	TC	Tmin/Tmax storage temp, no bias	100/300cyc required, 500cyc for info	11
	THuB	85C/85%RH, unbiased	2khr required for non-hermetic use	11

* package level stress requirements not shown here

Laser Reliability

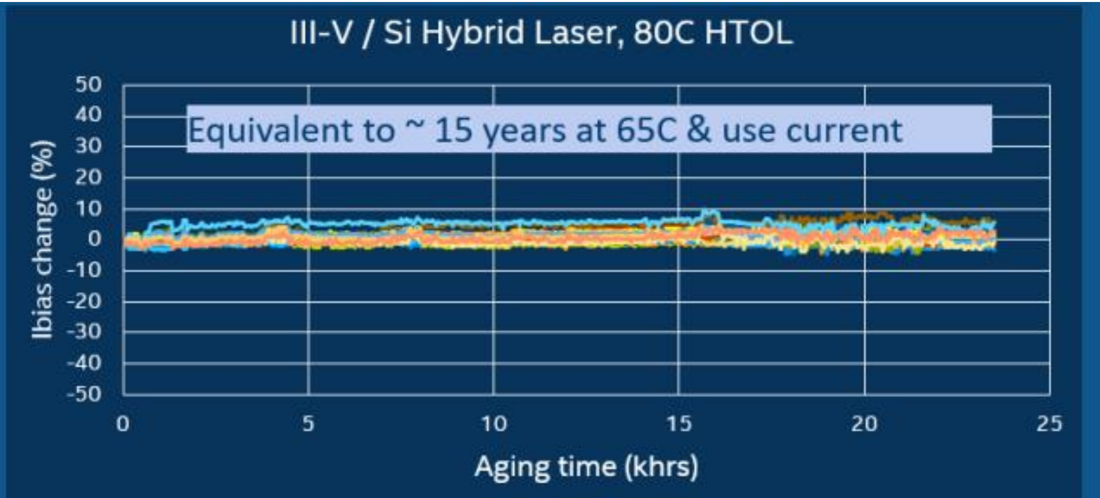
1) Device level (Low sample size, long duration)
   1) Thermal aging reliability model
   2) Telcordia HTOL
   3) Long term laser stability studies

2) Wafer level (high sample size, short duration)
   1) Early life/defect reliability for electrically and optically active process defects
   2) High volume data collection (10-100k lasers)
   3) Ongoing reliability monitoring

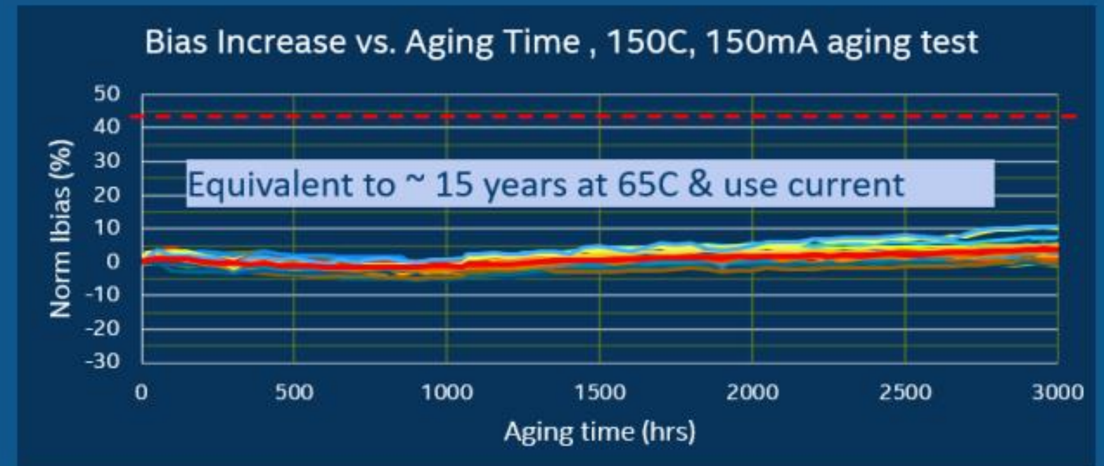
Laser failure rate ~2 FIT/Laser, validated with field data

Key modulators

- Temperature
- Current
- Optical power
- Mechanical strain



Long term HTOL study at max use condition



Accelerated Life Test

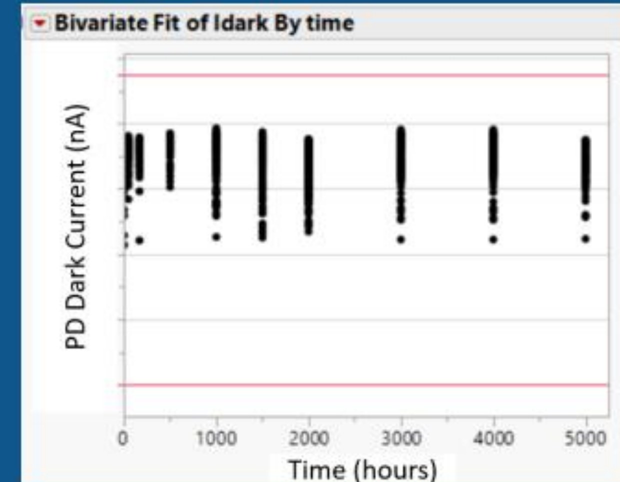
Photo Detector Reliability

- Key metrics:
  - Dark current (non-illuminated noise)
  - Responsivity (photo current)
  - Bandwidth (switching speed)

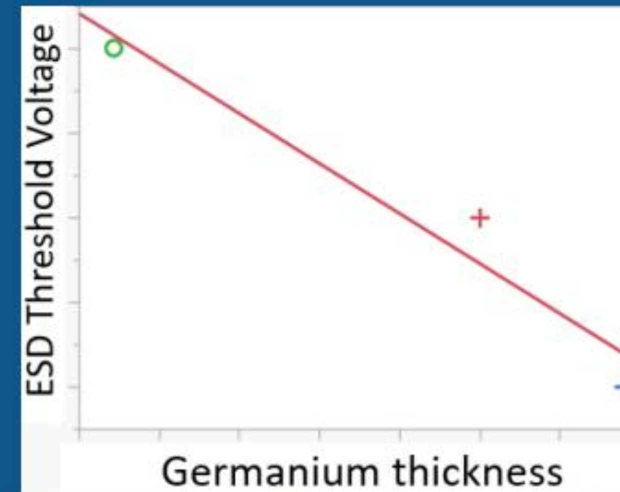
- PDs stressed up to 4x V_{use} (2x Telcordia requirement), no change observed over 5000 hours
  - Many packages cannot withstand 175ºC, done on PIC level

- Strongest signal: ESD (HBM) with threshold correlating inversely to thickness

100Gbps/lane PD FIT ~0.8 @ 65ºC, 90% CL



PD dark current, HTOL at 175ºC, 4xVuse



ESD threshold vs Germanium thickness

SiP Reliability Opportunities

Reliability Infrastructure

1) Gear toward turn-key reliability systems
2) Expanding test coverage for more info
3) Design for testing/stressing to obtain device rel data at product level

Reliability methodology

1) Supplement industry-standard-based with knowledge-based qualification to keep pace with innovation and new usage conditions for SiP

Technology

Advanced rel capabilities to address new introduction of IPs and integration schemes, for examples:

1) Light source options:
   a) Coupled external lasers and PICs
   b) Hybrid laser integration bonding scheme
   c) QD lasers
   d) Direct III-V materials grown on Si
2) Material systems:
   a) Various III-V systems

→ Exciting new areas for any reliability engineer!!!

Summary

- CPI is becoming a critical reliability issue due to adoption of advanced Si node and new packaging materials
- Many factors affect CPI failures, stresses and under bump metal structures are the key factors
- From IC product prospective, the conventional FEA approach is not adequate to address this reliability issue because it can’t simulate the real under bump structure
- TSV/u-bump integration added additional CPI failures
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