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Copper Braided Solder Columns – Extending Life in Space Applications

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Legacy copper wrapped solder columns are used to connect Field Programmable Gate Arrays (FPGA) and Application Specific Integrated Circuits (ASIC) chips to Printed Circuit Boards (PCB).

This heritage technology is approaching 40 years old, and is inherently limited in performance, especially concerning electrical impedance, thermal conductivity and operating life.

Problems with legacy copper wrapped columns are summarized as follows:

- If the single copper ribbon breaks, then the signal may encounter performance aberrations.

- Wrapped columns do not provide significant heat transfer from the underside of the chip to the PCB, requiring in some cases a top mounted heat sink, adding unnecessary size and mass.

- Electrical signals travel a long distance (6.7mm) along a wrapped helix copper path from the chip to the PCB.

- Chip package size is constrained by 1.0mm pitch due to the mechanical construction of copper wrapped solder columns.

To remedy the above problems, a new **Braided Solder Column** was invented.

Braided columns are constructed with 16 individual copper wires to create an exoskeleton conductive sleeve to provide a redundant signal path. If one wire strand breaks, then the remaining strands keep electrically connected.

Braided columns may provide up to 66% shorter signal path from the chip to the PCB through its copper conductor that is 2.5mm long instead of 6.7mm long found in legacy wrapped columns.

Braided columns potentially offer lower thermal impedance, possibly reducing the need for a heavy heat sink on top of the chip.

Braided columns provide a roadmap to reduce package size with 0.8mm pitch.

Engineering samples of braided columns are currently available.

Work to characterize braided columns is on-going.

Life-cycle testing at NASA Marshall Space Flight center is anticipated.

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